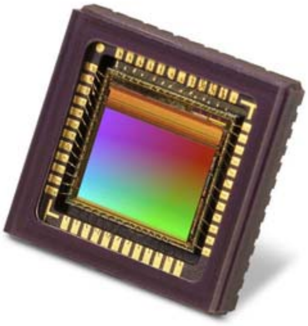
EV76C454
0.5 Mpixel Digital 1/2.9" CMOS Image Sensor

Datasheet

Features



- 0.5 Million Pixels, Low-light, Global Shutter CMOS Sensor
- 5.8 µm Square Pixels with Micro-lens
- Region of Interest Programmability:
  - Width, Height and Offset Adjustments
  - Subsampling
  - H and V Flips
- High Dynamic Range
- Single Master Clock Operation
  - Input Frequency 48 MHz
- Power Supplies 3.3V and 1.8V
- Low Power Consumption
- Output Format
  - Raw 8-bit Parallel
  - Separate 3 x 3 Filtered 8-bit
  - Sync (Frame, Line and Pixel Clocks)
- Two Wire Interface Control
  - Integration and Wait Time
  - Gain Analog and Digital
  - Trigger
  - Standby Mode
  - Line Length
  - Test Pattern
- Control Pins:
  - Trigger
  - TWI Address
  - Standby
  - Reset
- Operating Temperature [–30° to +65° C]
- Package:
  - µCLCC48 10 × 10 mm
  - RoHS Compliant

Applications

- Surveillance IP/CCTV Cameras ; Industrial Machine Vision
- Biometrics/Medical Imaging ; Automotive Vision

Visit our website: www.e2v.com
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e2v semiconductors SAS 2009

Introduction

This 0.5 million pixel CMOS image sensor designed on e2v's proprietary *eye-on-Si* CMOS imaging technology is ideal for diverse applications where superior performance is required. Its innovative pixel design offers excellent performance in low-light conditions with an electronic global (true snapshot) shutter, and offers a high-readout speed at 60 fps in full resolution, and 80 fps in VGA mode. Very low power consumption enables this device to be used in battery powered applications.

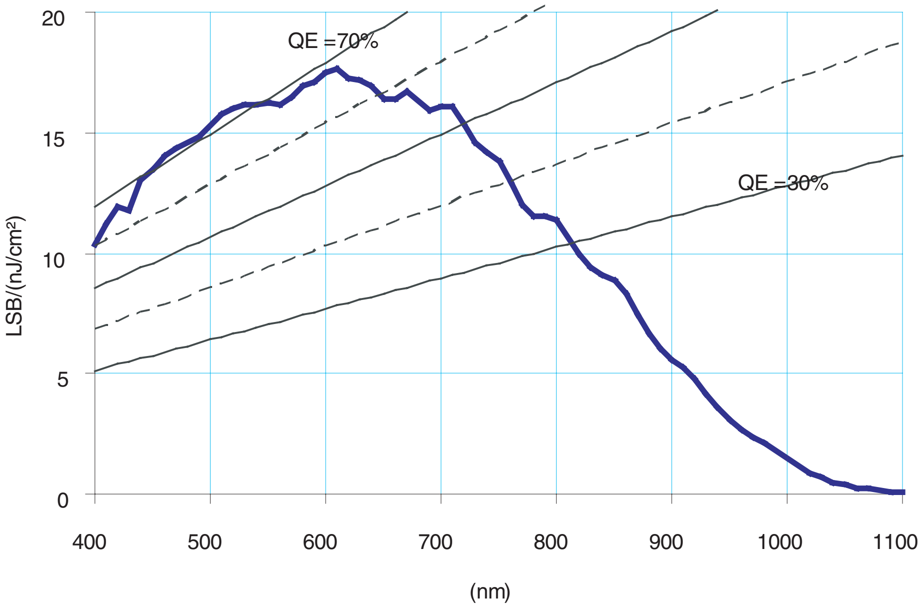
1. Typical Performance

Table 1-1. Electro-optical Performances

Sensor Characteristics	Value	Unit
Resolution	838 (H) × 640 (V)	Pixels
Image size	4.9 (H) × 3.7 (V) 6.1 (diagonal) 1/2.9	mm mm Inches
Pixel size	5.8 × 5.8	(square) µm
Aspect ratio	4/3	
Max frame rate	60 @ Full format 80 @ VGA format	fps
Pixel rate	48	Mpixels/s
Pixel Performance		
Bit depth	8	Bits
Dynamic range	> 51	dB
Qsat	10	ke$^-$
SNR Max	40	dB
MTF at Nyquist, λ = 650 nm	50	%
Dark signal[1]	8	LSB$_8$/s
DSNU[1]	6	LSB$_8$/s
PRNU[2](RMS)	0.8	%
Responsivity[3]	17	LSB$_8$/(nJ/cm^2)
Mechanical and Electrical Interface		
Power Supplies	3.3 and 1.8	V
Power consumption Functional[4] Standby	 80 90	 mW µW

Notes:
1. @ 25° C, min gain, 8 bits.
2. measured @Vsat/2, min gain.
3. 670 nm, window without AR coating.
4. @ 60 fps and full format and with 10 pF on each output.

Figure 1-1. Spectral Response and Quantum Efficiency Gain = 1



2. Warnings

2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings

VDD18A and VDD18D supply voltage	–0.3V; 2.2V
VDD33A supply voltage	–0.3V; 3.9V
DC voltage at any “Dig IN” input pin	–0.3V, VDD18D + 0.3V
DC Voltage at “Ana IN” input pin	–0.3V; VDD33A + 0.3V
DC voltage at “TWI” pin	–0.3V; 3.9V
Storage temperature	–40° C to +85° C
Operating temperature	–30°C to +65° C
(see Section 15. for input/output type)	

- Stresses above those listed under **Section 2-1** might cause permanent device failure.
- Operating at or above these limits should be avoided. Exposure to absolute maximum ratings for extended periods might affect reliability.
- All power pins with the same name must be connected to the same power supply. All grounds must be connected.

2.2 ESD

The EV76C454 is sensitive to ESD (electrostatic discharge). In order to avoid accumulation of charges and to prevent electrical field formation, the following precautions must be taken during manipulation:

- Wear anti-static gloves or finger cots, anti-static clothes and shoes
- Protect workstation with a conductive ground sheet
- Use conductive boxes

2.3 Cleaning the Window

The EV76C454 sensor is an optical device. All precautions must be taken to prevent dust or scratches on the input window.

If cleaning the windows is needed, use the following procedure:

2.3.1 Equipment

- Ethanol
- Wipe, optical paper, cotton buds
- Filtered blow-off gun (preferably with static charges neutralizing device)
- Area protected versus electrostatic discharges and equipped with ground straps

2.3.2 Preparations

- Wear vinyl gloves or finger cots without talcum powder
- Make use of anti-ESD equipment: ground straps, ionisers etc.

2.3.3 Recommendations

- Never dry clean
- Soak the cleaning medium with alcohol and do not pour it directly on the windows
- Clean the windows only if necessary

2.3.4 Operating Procedure

- Air-jet cleaning of the glass window
- If stains or dust remain:
  - Soak the cleaning medium with alcohol and move it in a single movement from one side to another
  - Always use a clean part of the cleaning medium for a new attempt
  - Fit the sliding speed to let alcohol evaporate without leaving traces
  - Eventually blow the windows off another time

3. Standard Configuration

3.1 Electrical Levels

To be ready to use, the sensor should be connected as follows:

- All grounds should be connected (see Section 15.1)
- Power on 3.3V and 1.8V pins. Note that EV76C454 is sensitive to power supply noise. Special care must be taken to power supply bypassing and on power supply generator noise
- ResetB pin at high level

- Standby pin at low level. (The sensor leaves the standby mode if this pin and the standby TWI bit are correctly configured)
  - CLKREF input pin is fed with a clock (nominal value is 48 MHz)
  - TRIG input pin tied to low level if trigger mode is controlled by soft
  - TWI (two wire interface) signals SDA (serial data) and SCL (serial clock) connected to the host controller with the proper pull-up resistors

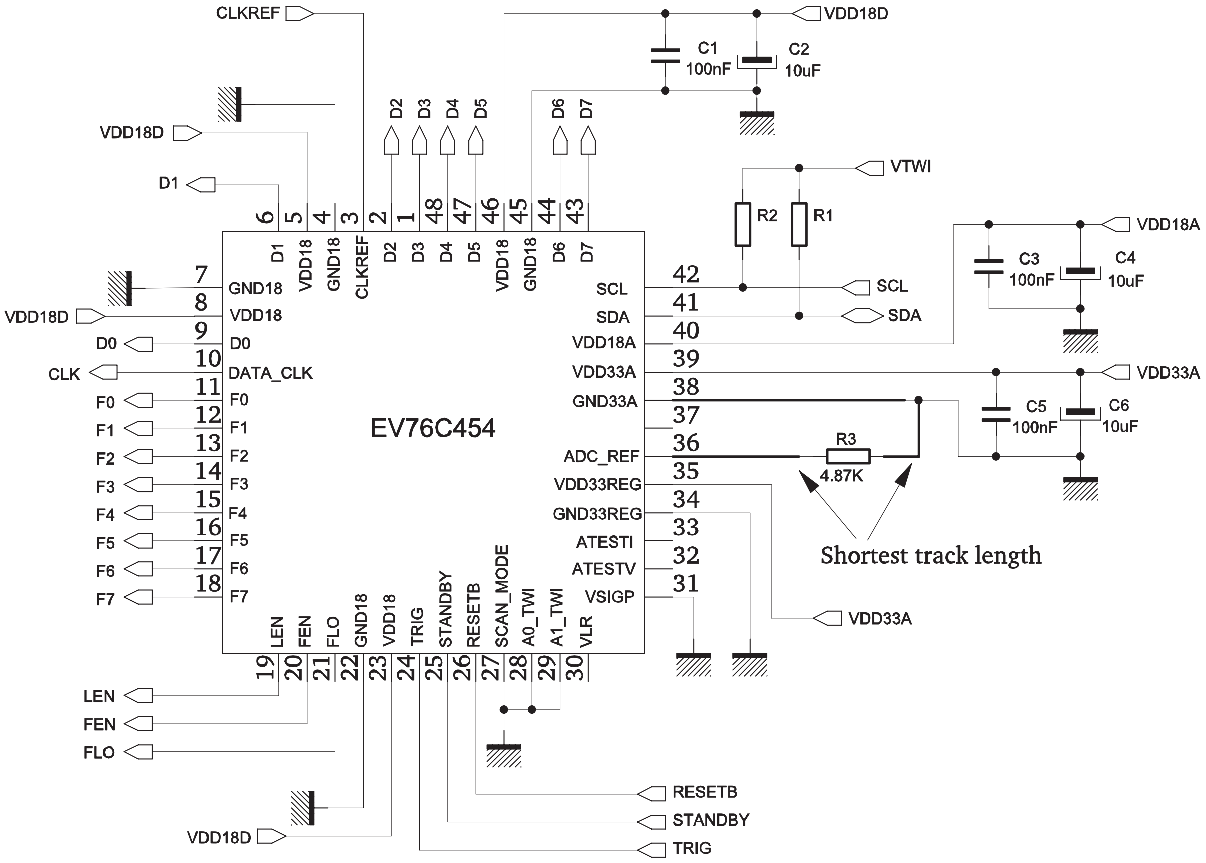
For more information on timings (see Section 9.9.7).

Table 3-1. Sensor Settings

Pin Number	Name	Connections and Bypass Recommendations
5	VDD18D	1.8 V + 100nF + 10 µF
8	VDD18D	1.8 V + 100nF + 10 µF
23	VDD18D	1.8 V + 100nF + 10 µF
27	SCAN_MODE	Ground
28	A0_TWI	0 or 1.8V No internal pull up or pull down
29	A1_TWI	0 or 1.8V No internal pull up or pull down
30	VLR	DNC
31	VSIGP	Ground
32	ATESTV	DNC
33	ATESTI	DNC
35	VDD33A	3.3 V + 100nF + 10 µF
36	ADC_REF	External resistor between this pin and ground. For value see Section 6.2. The ground connection should be as short as possible to the sensor.
39	VDD33A	3.3 V + 100nF + 10 µF
40	VDD18A	1.8 V + 100 nF + 10 µF
41	SDA	External pull up
42	SCL	External pull up
46	VDD18D	1.8 V + 100nF + 10 µF

Note: DNC stands for do not connect.

Figure 3-1. Typical Schematic



4. Sensor Architecture

Figure 4-1. Block Diagram

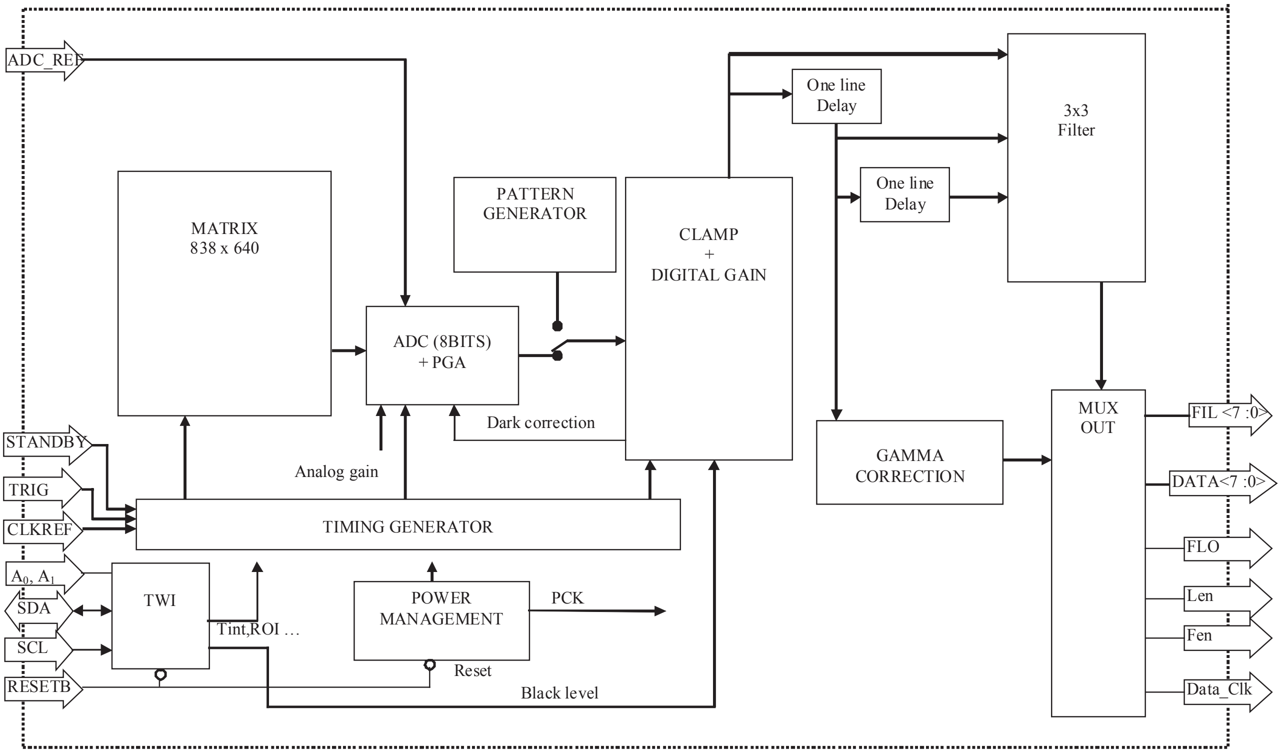


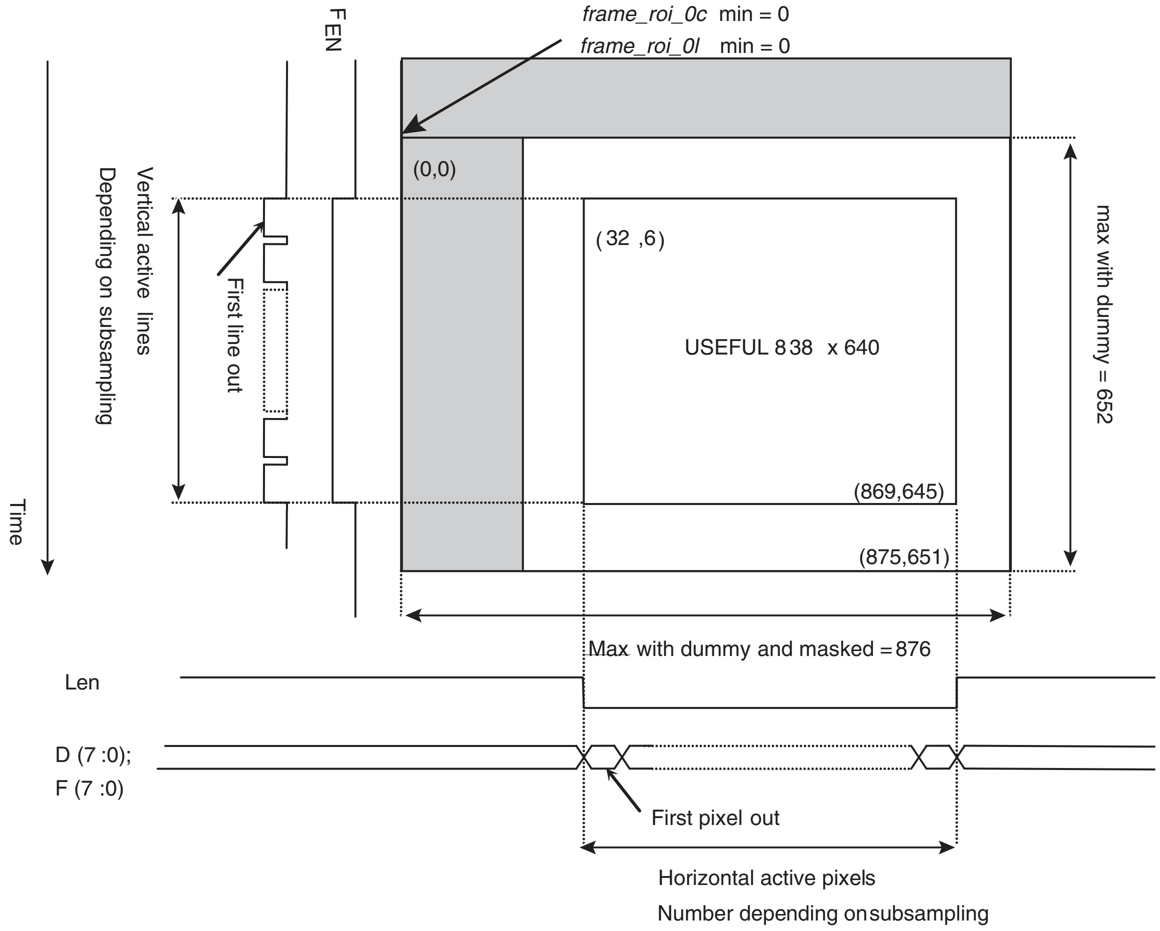
Table 4-1. Input and Output List – Block Description

Name	I/O	Detailed Pinout Information (see Section 15.1)	Notes	Blocks list	Notes
ADC_REF	I	Adjust the conversion range. Connected to GND through a resistor	Section 6.1	Matrix	Section 5.
ResetB	I	Reset the sensor. The internal registers are set at default values		ADC + PGA	Section 6.
Standby	I	A high level puts the sensor in standby mode	Section 11.2	Clamp + digital gain	Section 7.
TRIG	I	A high level starts the image capture	Section 9.5	Pattern generator	Section 8.
CLKREF	I	Reference clock input	Section 11.1	Timing generator	Section 9.
A<1:0>	I	2 LSB TWI address *warning* no pull up or pull down included	Section 10.1	TWI	Section 10.
SDA	I/O	TWI data pad, open drain access, should be tied with a pull-up resistor	Section 10.5	Power management	Section 11.
SCL	I	TWI clock input (400 kHz)	Section 14.2	3x3 filter	Section 12.
DATA<7:0>	O	Data out bus		Gamma correction	Section 13.
FIL<7:0>	O	Filter out bus		Mux out	Section 14.
DATA_CLK	O	Output clock			
FEN	O	Vertical synchronization output			
LEN	O	Horizontal synchronization output			
FLO	O	External illumination control output			

5. Matrix

5.1 Sensor Frame Structure

Figure 5-1. Matrix Structure



Note: Digital address of first pixel from useful area is 32 (H), 6 (V).
Twenty six columns are optically masked.

5.2 Pixel

Pixel size 5.8 µm × 5.8 µm. Global shutter is performed thanks to 5T pixels allowing integration during the readout.

5.3 ROI

The region of interest might be chosen to output only data from the needed area.

Four TWI registers might be used:

- Address of first column: *frame_roi_0c* (see Section 10.4.2.4)
- Address of first line: *frame_roi_0l* (see Section 10.4.2.5)
- Width of the ROI: *frame_roi_w* (see Section 10.4.2.6)
- Height of the ROI: *frame_roi_h* (see Section 10.4.2.7)

5.4 Flip

To allow using lens with mirror, flip functions are embedded in the sensor. The flip function allows reading the defined ROI from top to bottom, bottom to top, right to left or left to right. Combining horizontal and vertical flip is a 180° rotation.

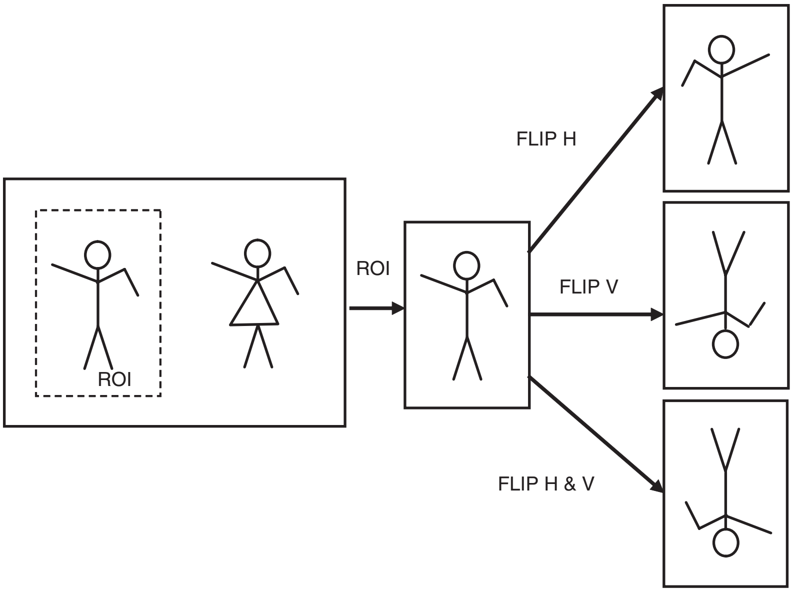
Table 5-1. Flip H and V Starting and Ending Points

	Reading	From	To
No H flip	*frame_cfg_fliph* = 0	*frame_roi_0c*	*frame_roi_0c* + *frame_roi_w* –1
With H flip	*frame_cfg_fliph* = 1	*frame_roi_0c* + *frame_roi_w* –1	*frame_roi_0c*
No V Flip	*frame_cfg_flipv* = 0	*frame_roi_0l*	*frame_roi_0l* +*frame_roi_h* –1
With V flip	*frame_cfg_flipv* = 1	*frame_roi_0l* + *frame_roi_h* –1	*frame_roi_0l*

frame_cfg_flipv & frame_cfg_fliph, (see Section 10.4.1.4).

5.4.1 Example of Flips

Figure 5-2. Flip H & V Example



5.4.2 Color and Address of Pixel Using Flip(s) in Full ROI in WRGB CFA Option

Figure 5-3. First Pixel Address with WRGB CFA

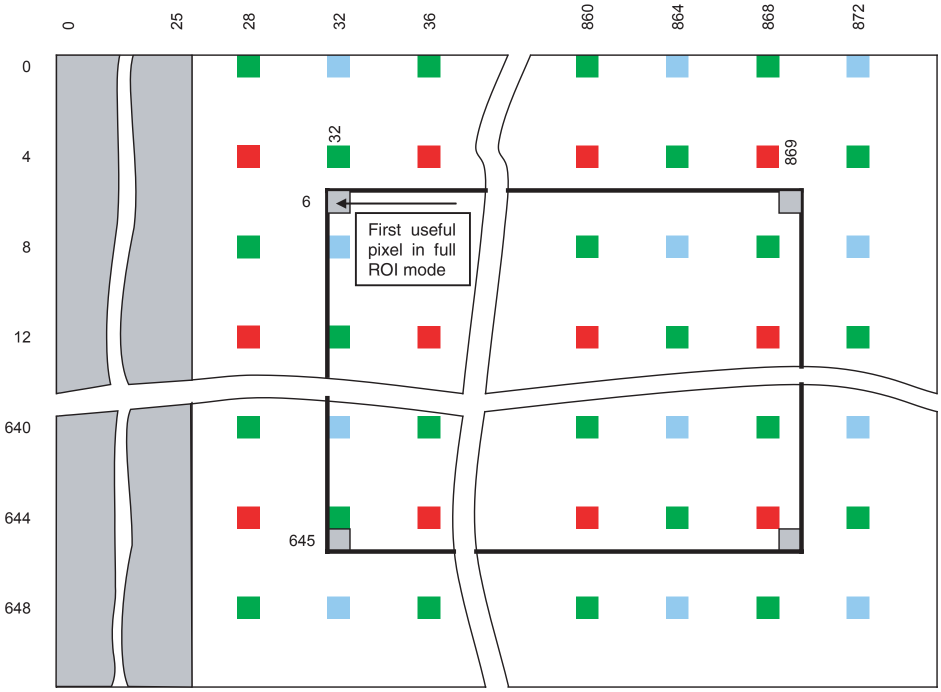


Table 5-2. Color and Address of First Colored Pixel with WRGB CFA Option

	First Useful Colored Pixel	
	Color	**Address (H,V)**
No Flip	Blue	32, 8
Flip H	Green Blue	868, 8
Flip V	Green Red	32, 644
Flip H & V	Red	868, 644

5.4.3 Color and Address of Pixel Using Flip(s) in Full ROI in Bayer CFA Option

Figure 5-4. First Pixel Address with RGB Bayer CFA

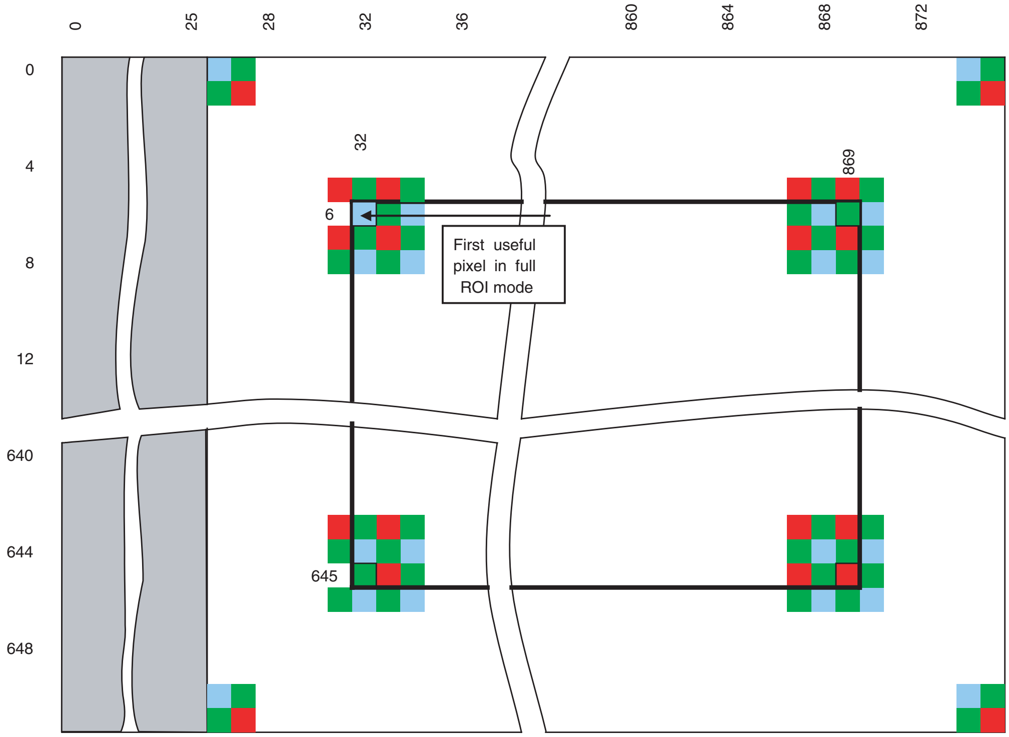


Table 5-3. Color and Address of First Colored Pixel with Bayer CFA Option

	First Useful Colored Pixel	
	Color	**Address (H,V)**
No Flip	Blue	32, 6
Flip H	Green Blue	869, 6
Flip V	Green Red	32, 645
Flip H & V	Red	869, 645

5.4.4 Address of Pixel Using Flip(s) in Full ROI in Black and White Option

Figure 5-5. First Pixel Address of Pixel Using Flip(s) in Full ROI

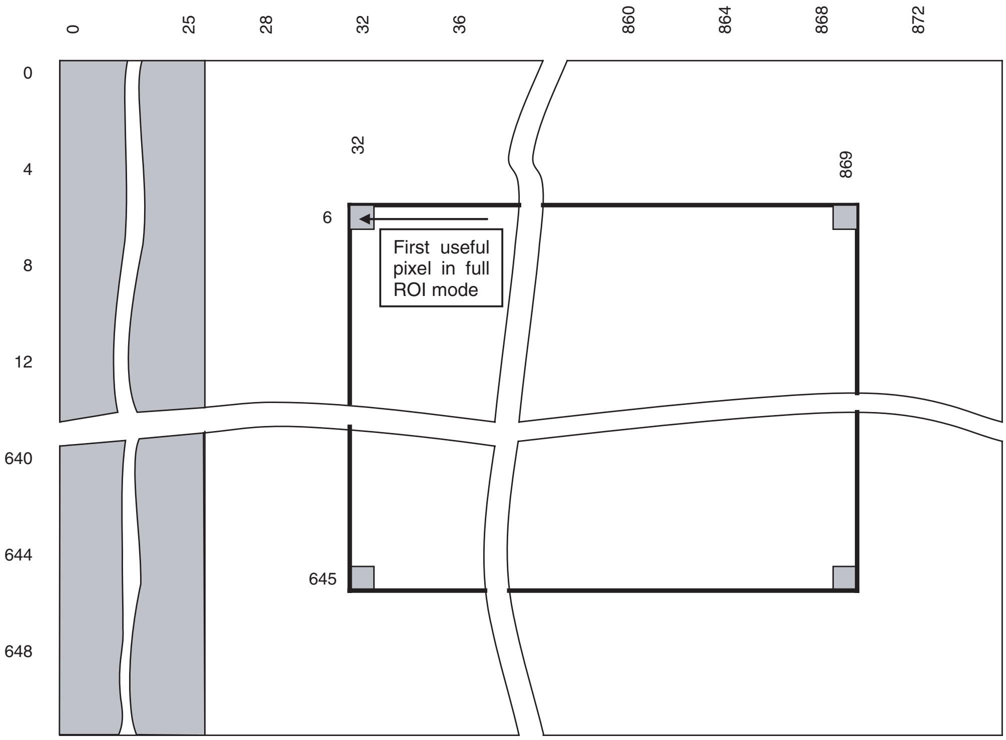


Table 5-4. Address of First Pixel with Black and White Option

	First Useful Pixel Address (H,V) (Col, Row)
No Flip	32, 6
Flip H	869, 6
Flip V	32, 645
Flip H & V	869, 645

5.5 Subsampling

A subsampling factor can be used for image readout. See *frame_cfg_subsfactor[2:0]* Section 10.4.1.4. Subsampling factor 1, 2, 4, 8 or 16 allow respectively to read one pixel out of 1, 2, 4, 8 or 16 pixel(s) and out of 1, 2, 4, 8 or 16 line(s). The same factor is applied in both directions.

This subsampling function allows a gain in the frame rate. This gain is in the ratio of subsampling. For example the frame readout period is divided by 4 if 1 out of 4 subsampling factor is used.

This subsampling function can be used in conjunction with the ROI function. For example using 1 out of 4 subsampling factor *frame_cfg_subsfactor[2:0]* = 2 and *frame_roi_0c = 8*, *frame_roi_0l = 32, frame_roi_w = 640, frame_roi_h* = 480 will give a QQVGA output format.

5.6 Log Function

The logarithmic response of the pixel can be adjusted: *frame_vlr_ctrl (*see Section 10.4.1.5).

To get a logarithmic response gain 1 must be used: *frame_gain_analog* (see Section 10.4.2.3). A linear response is also set by frame_vlr_ctrl[3:0]=1.

5.6.1 Possible Adjustments

When the log mode is used the transfer function of a device is depending on:

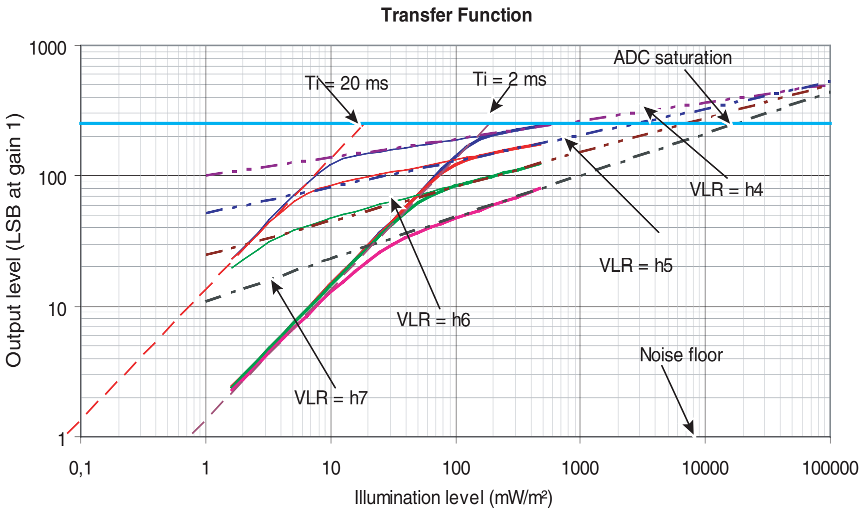
- The VLR (low voltage of the reset signal at pixel level)
- The integration time; one may note that this transfer function is versus power illumination per area unit and not versus energy per area unit

5.6.2 Linear and Logarithmic Transfer Function Example

On Figure 5-6 the measured curves at 2 ms and 20 ms integration time are drawn for four different VLR adjustments. The asymptotes (in Lin and in Log mode were added).

The following curves are at Gain 1, λ = 670 nm (40 nm width), room temperature, nominal power supply values, on a 100 × 100 pixel centered area.

Figure 5-6. Transfer Response Examples



The maximum accessible dynamics are depending on the two parameter choices.

Table 5-5. Dynamic Max In Lin/Log Mode

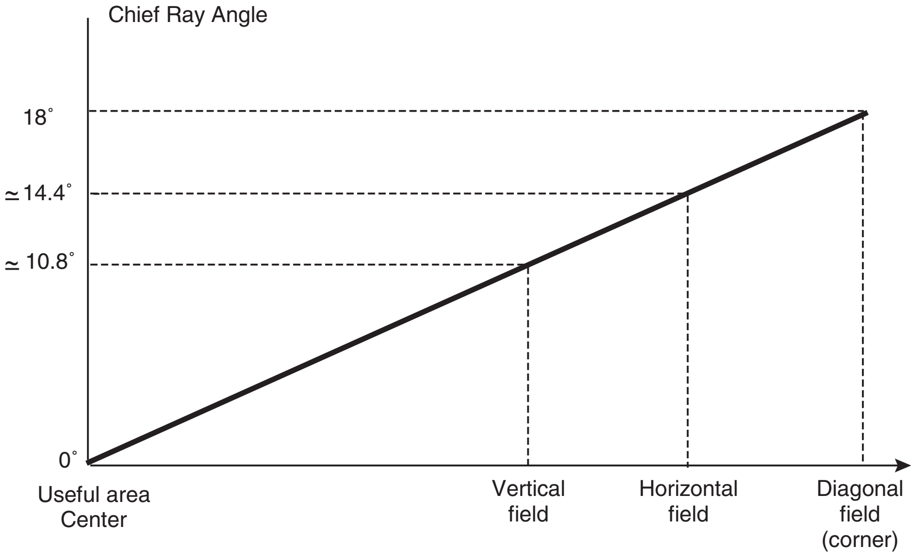
VLR	Dynamic Max (dB)	
	Tint = 2 ms	Tint = 20 ms
4	47	65
5	74	93
6	85	104
7	92	111

Note: These values are given as examples. Real results might vary from one device to another, *frame_vlr_ctrl* adjusts part of response in log versus part of linear response, (see Section 10.4.1.5).

5.7 Chief Ray Angle Compensation

The sensor has been designed to compensate linearly the lens' CRA. This compensation is centered on the useful area and is optimized for a maximum CRA of 18° in the corners.

Figure 5-7. CRA Compensation



5.8 Output Data

EV76C454 has two sets of synchronous 8-bit data outputs.

5.8.1 Standard Data

Output is raw data. The clamp might be used to restore the DC output level. Gain should be adjusted, (see Section 7.).

5.8.2 Filtered Output

A 3x3 filter might be added, (see Section 12.).

6. ADC + PGA

6.1 Analog-to-digital Conversion

A slope ADC is embedded in the sensor. All pixels of one line are converted at the same time.

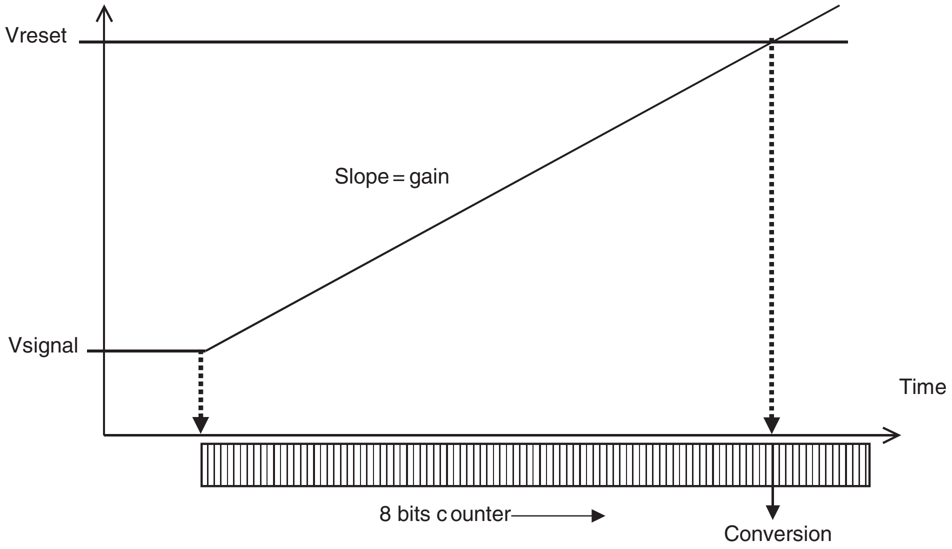
For conversion:

- A slope and a counter are internally generated
- Each analog pixel value is compared to the slope value. When the pixel and the slope have the same value the counter value is stored in a memory.

To adjust the slope rate (conversion gain or gain 1 value) an external resistor (see Section 6.2) must be used. The precision of the resistor value gives the precision of the gain conversion. We recommend using a 1% precision resistor.

Note that any variation of the counter frequency (directly linked to the external master clock) will introduce a gain variation and so temporal noise.

Figure 6-1. Slope ADC



6.2 External Resistor

A 1% resistor should be connected externally between the ADC_REF pin and ground. Internal impedance is few hundred Ohms.

The external resistor value depends on the master clock frequency and on the ADC saturation choice in analog gain 1.

$$R_{ext} = \frac{K}{CLKRE \times V_{sat}} - 600 \qquad K = 171.4 \quad 10^9$$

With:

- CLKREF = 48 MHz
- V_{sat} = 650 mV

Rext = 4.87 kΩ (1% standard nearest value) must be used.

6.3 Programmable Gain Amplifier

Analog gain is controlled by *frame_gain_analog* (see Section 10.4.2.3.)

Table 6-1. Analog Gains

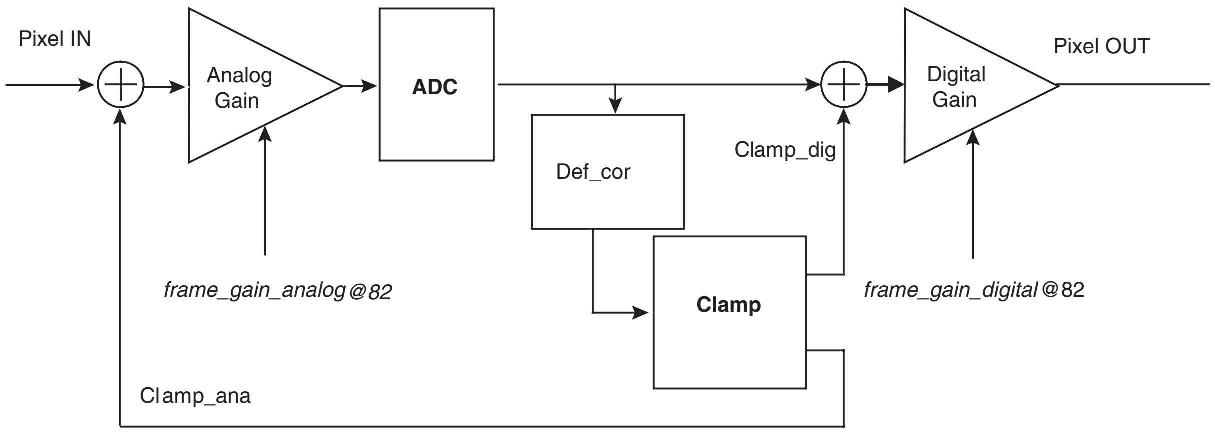
Analog Gains	
G<2:0> code	Gain Value
000	1
001	1.5
010	2
011	3
100	4
101	6
110 and 111	8

Note: These values are relative values. Gain 1 absolute value is adjusted by the external resistor.

7. Clamp + Gain

7.1 Clamp Principle

Figure 7-1.



The EV76C454's clamp is performed using an analog method (Clamp_ana in Figure 7-1.) If the needed correction is above the maximum analog range correction, a digital subtraction is added (Clamp_dig in Figure 7-1).

After the ADC, during the beginning of readout (before useful pixels), reference pixels are:

- Filtered (any white pixel is removed through a median filter)
- Averaged
- Compared to previous value using a threshold value:
  – *clamp_thld_lock[3:0]* is used to adjust the threshold value (see Section 10.4.1.13).
  – *clamp_locker_ena* disable the use of the threshold (see Section 10.4.1.13).

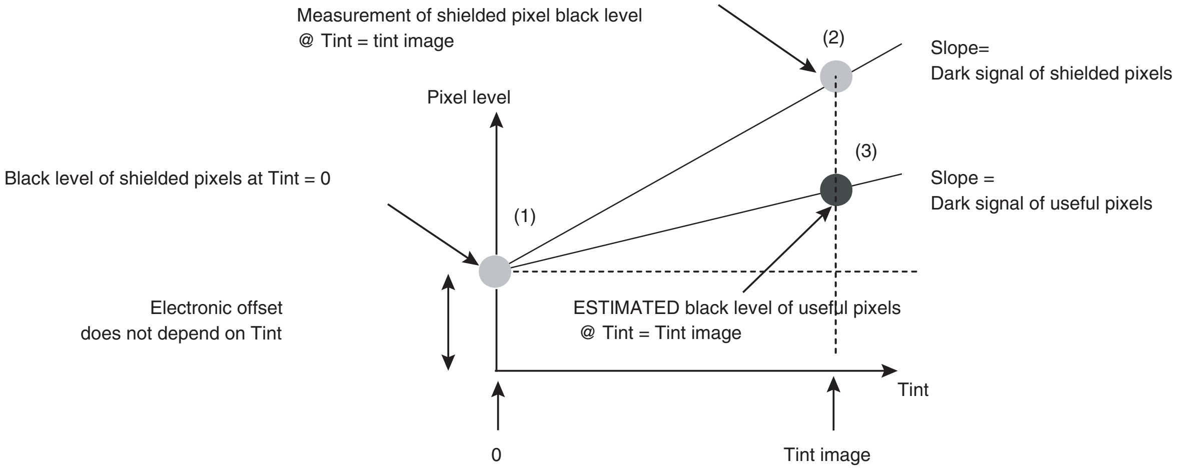
If the new value is close to the previous value nothing is changed. (This enables a good stability on the image in a video mode).

If a change has been detected the new value is used to correct the following image. Corrected clamp is also applied whenever gain or integration time has changed according to previous frame.

7.2 Clamp Function

In order to compensate possible difference in dark current generation between masked pixel and useful pixels, the clamp works as follows:

Figure 7-2. Clamp Principle


Measurement of shielded pixel black level
@ Tint = tint image
(2)
Slope=
Dark signal of shielded pixels
Pixel level
(3)
Black level of shielded pixels at Tint = 0
Slope =
Dark signal of useful pixels
(1)
Electronic offset
does not depend on Tint
ESTIMATED black level of useful pixels
@ Tint = Tint image
Tint
0
Tint image

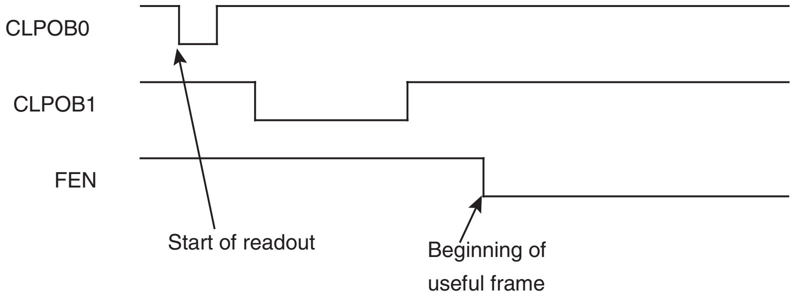
The clamp:

- Acquire the signal processing channel offset, see Figure 7-2 step(1)
- Acquire the dark signal mean value of masked pixel, see Figure 7-2 step(2)
- Compute the dark signal of useful pixel by applying a gain (V0_Gain), see Figure 7-2 step(3)

All the dark signal acquisition and computation are performed before outputting the data:

- CLPOB0 is used to compute Clamp_0 (offset of the signal processing channel)
- CLPOB1 is used to compute Clamp_1 (mean value of masked pixels includes offset)

Figure 7-3. Clamp Timing



V0_gain value can vary. A typical value is 0.36.

To compute a more precise value one solution is to compute the mean non saturated value of images in darkness at two integration times (Tint1 & Tint2) and two V0_Gain values (V0_Gain_1 & V0_Gain_2).

If we call:

- K1 the mean value of image obtained with integration time Tint1 and V0_Gain_1
- K2 the mean value of image obtained with integration time Tint1 and V0_Gain_2
- K3 the mean value of image obtained with integration time Tint2 and V0_Gain_1
- K4 the mean value of image obtained with integration time Tint2 and V0_Gain_2

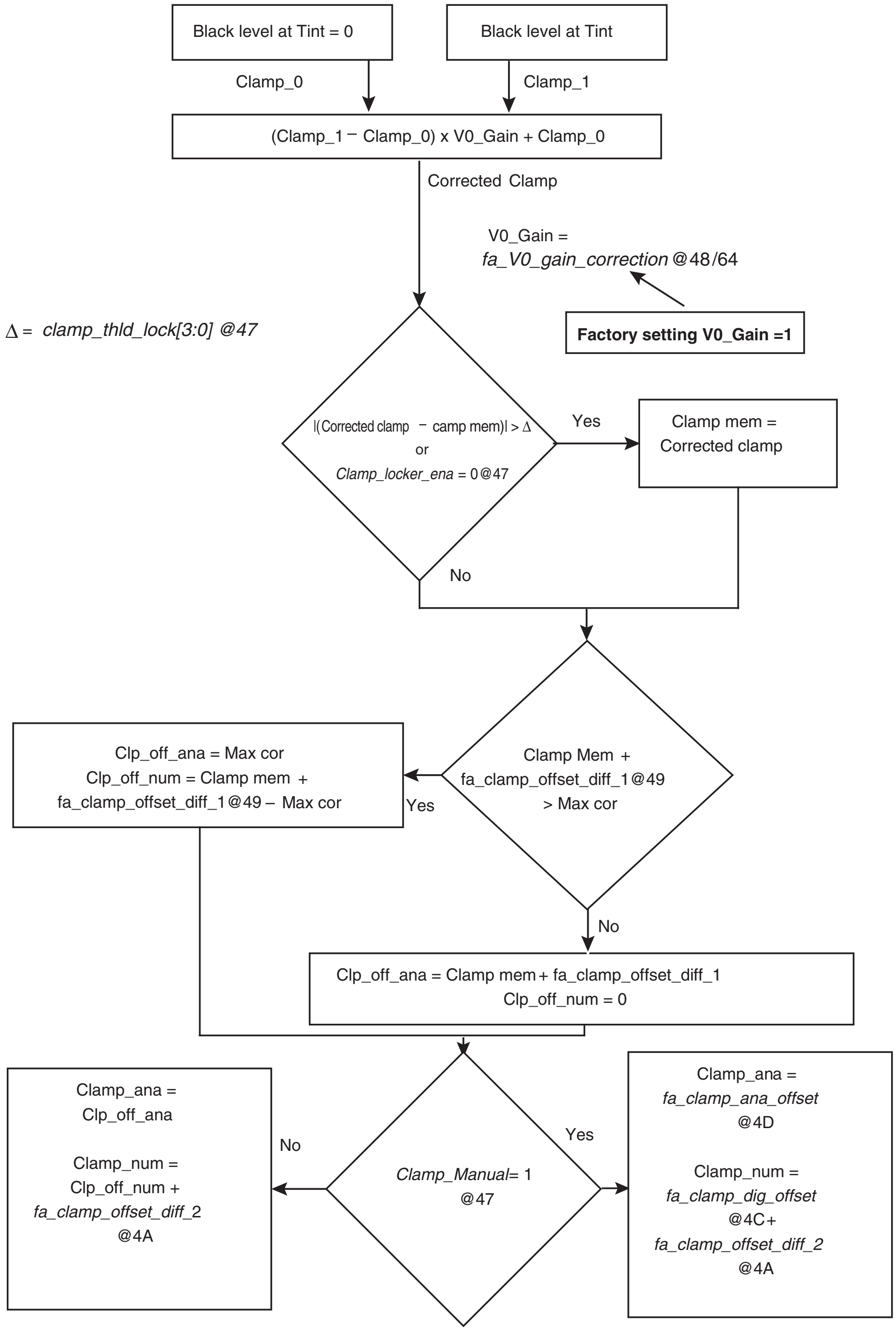
The V0_gain to be applied is computed by:

$$\text{V0\_Gain} = \frac{\text{V0\_Gain}_2 \times K_1 - \text{V0\_Gain}_1 \times K_2 - \text{V0\_Gain}_2 \times K_3 + \text{G0\_Gain}_1 \times K_4}{K_1 - K_2 - K_3 + K_4}$$

clamp_v0_gain_correction[5:0] = 64 × V0_Gain (see Section 10.4.1.14.).

7.3 Clamp Algorithm

Figure 7-4.



It is recommended to use in priority analog offset by using *clamp_ana_offset[7:0]* see Section 10.4.1.17 (beware limit is d160).

7.4 Digital Gain

A digital gain can also be used in combination with analog gain (see Section 10.4.2.3).

8. Pattern Generator

In order to test the electronic part of the system using the sensor post optical section (light, lens etc.) a test pattern is included in the sensor.

Register: *pattern_ena* (see Section 10.4.1.12).

8.1 Video Output

pattern_ena = 00

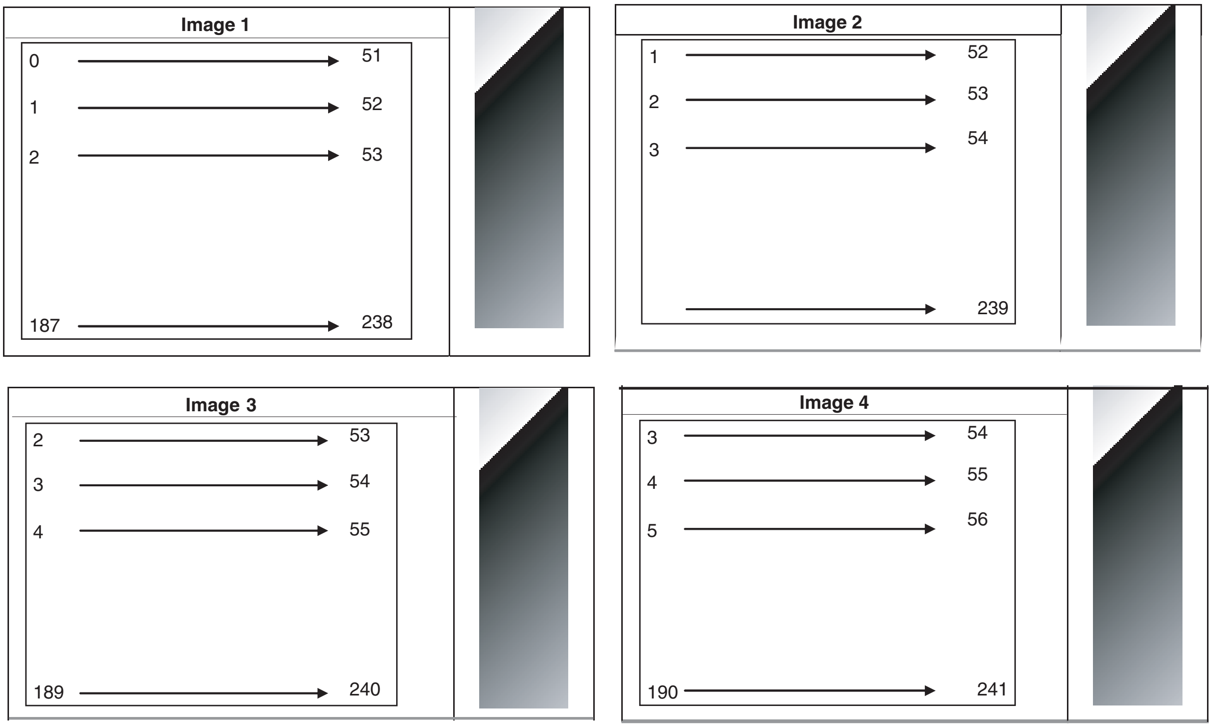
No test pattern: the video coming from the sensor array is output.

8.2 Moving Test Pattern

pattern_ena = 01

In this mode, the test pattern changes from line to line and from frame to frame. Examples are given for a ROI (52 × 188 pixels). If the ROI width or height are larger than 256 the test pattern counter will create additional ramp pulses in both directions.

Figure 8-1. Moving Test Pattern

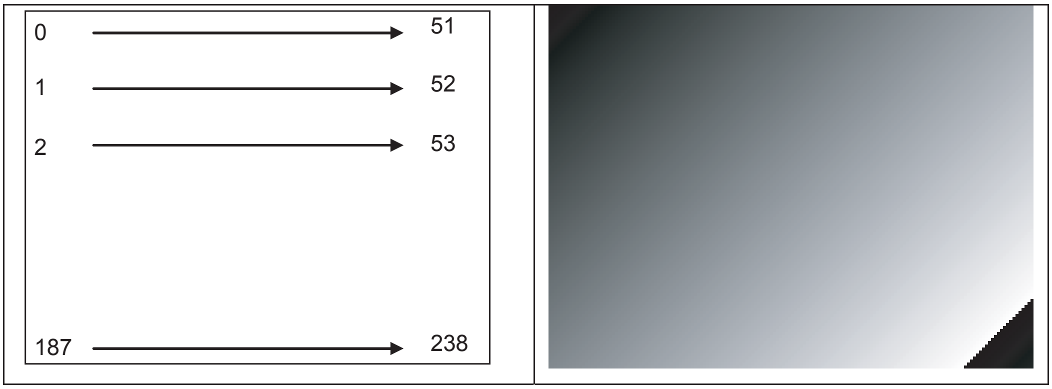


8.3 Fixed Test Pattern

pattern_ena = 10

Again using the same resolution example the test pattern ramp generator will always have the same starting point at 0 at the first pixel of first line.

Figure 8-2. Fixed Test Pattern



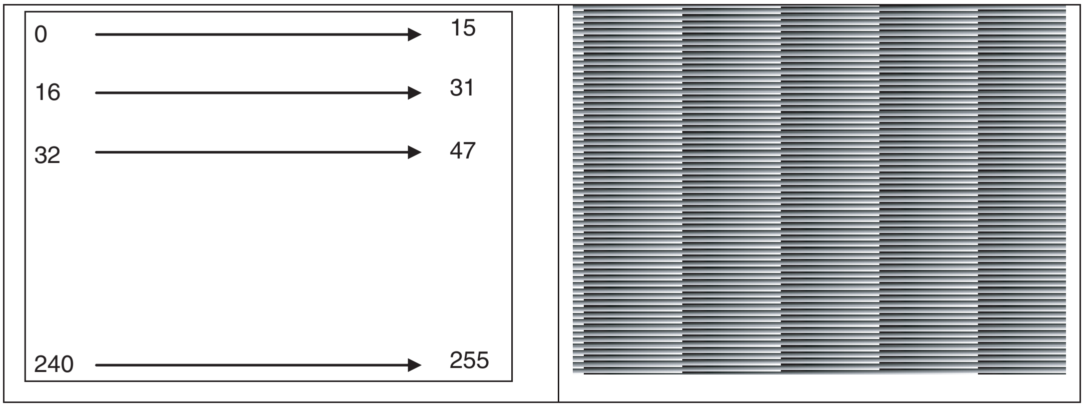
8.4 Functional Test Pattern

pattern_ena = 11

This test pattern allows all output values to occur in the smallest possible image. The test pattern counter counts only during active FEN & LEN. The first pixel of first line is at 0.

For example on a 16 × 16 image:

Figure 8-3. Functional Test Pattern



9. Timing Generator

Some other functions managed by the timing generator are described in other sections of this document. For example ROI management, subsampling etc.

9.1 Reset

An external signal can be applied on the reset pin. This will put the sensor back to the factory settings. Minimum pulse duration is 20 ns.

9.2 Synchronization Output Polarity

All the synchronization outputs might be in either normal or inverted polarity, DATA_CLOCK, LEN, FEN and Flash output (FLO) *dataclk_inv, sync_fen_inv, sync_len_inv & sync_flash_inv* (see Section 10.4.1.3). In all the timing diagrams, these signals are shown non-inverted.

9.3 Mask

LEN might be active/enabled or not when FEN is inactive (see Section 10.4.1.3) and data might be stuck at 0 when FEN is inactive, (see Section 10.4.1.3).

9.4 Flash Control

Three TWI registers are used for controlling the FLO (Flash Output) signal. The output signal might or might not be inverted. (This signal is always non-inverted in the timing diagrams). Sync_flash_inv (see Section 10.4.1.3).

The FLO signal might be enabled/disabled, and its delay can be adjusted. Flash_disa & frame_flash_del (see Section 10.4.1.6).

The FLO falling edge is synchronous with the integration time end, that is FL_width = Tint + FL_DEL.

9.5 Trigger

The sensor can be triggered either through an external pin *or* through a TWI register. Both signals have the same effect.

9.5.1 Trigger Input Control

To take into account a hardware trig signal, the TRIG pin must be enabled. It can be active at high or low level. Minimum width is 20 master clock periods.

Pad_trig_ena & pad_trig_inv control the trigger pin (see Section 10.4.1.7). The trigger pin can be left unconnected. An internal pull up ties it to high level so that the sensor grabs images when the TWI bits *trig and stdby_rqst* are high.

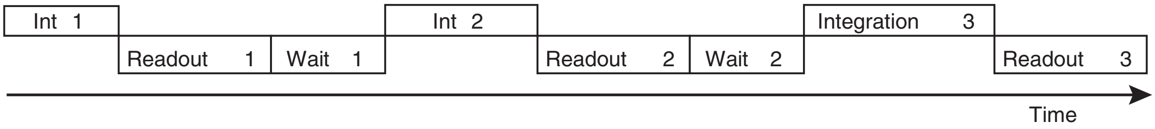
9.5.2 Trigger Through TWI

A trigger event through TWI or TRIG pin should be used in the same way, (see Section 10.4.1.8). A rising edge on this signal starts the integration of an image. Keeping this signal at an active level will put the sensor in the free running mode.

9.6 Serial/Overlap

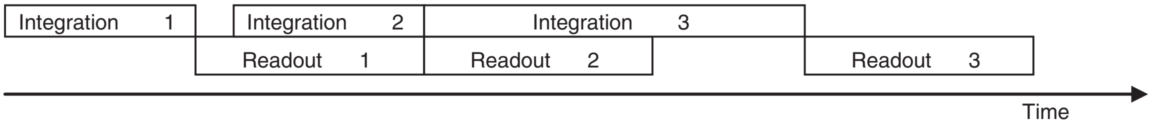
The choice of integrating during readout or not is controlled by the TWI register *overlap* (see Section 10.4.1.8). **In serial mode**, integration and readout are as follows:

Figure 9-1. Serial Mode



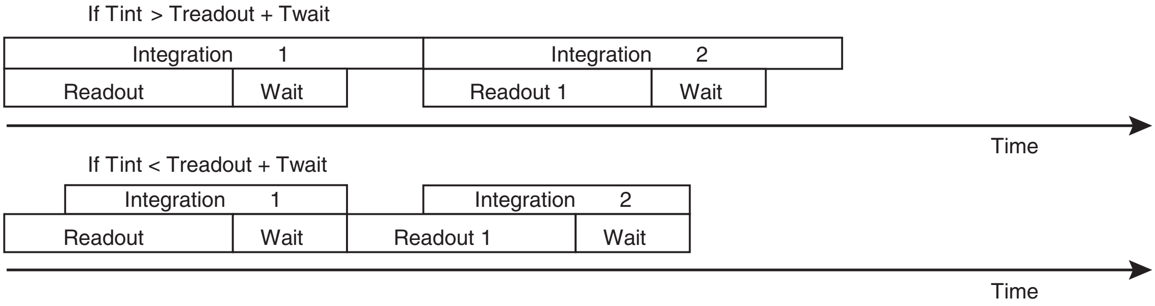
In overlap mode with no waiting time, integration and readout are as follows:

Figure 9-2. Overlap Mode



In overlap mode with a waiting time, integration and readout are as follows:

Figure 9-3. Overlap Mode with Twait



9.7 Abort Process

Abort is under control of the TWI register *mlbx_abort_data[1:0]* (see Section 10.4.1.9). Writing (any value) to *mlbx_abort_data*, triggers the *abort* process and sets the mailbox flag high. This flag is automatically reset at the end of the abort process.

During readout, the abort forces the sensor to only end the readout of current line and allows a new integration time to start (all remaining lines are lost, (see Section 9-13).

During integration time if an abort is launched, the timing generator will finish the current line (even if there is no LEN output). Then a new integration time will start. If a standby is requested before the abort then at the end of abort sequence the device will be put in standby mode.

9.8 Line Length Adjustment

If time is needed between two lines, the line length can be adjusted through TWI registers:

use_ext_line_length & line_length (see Section 10.4.2.9).

Note that using the line length adjustment impacts:

- Minimum integration time
- Frame period

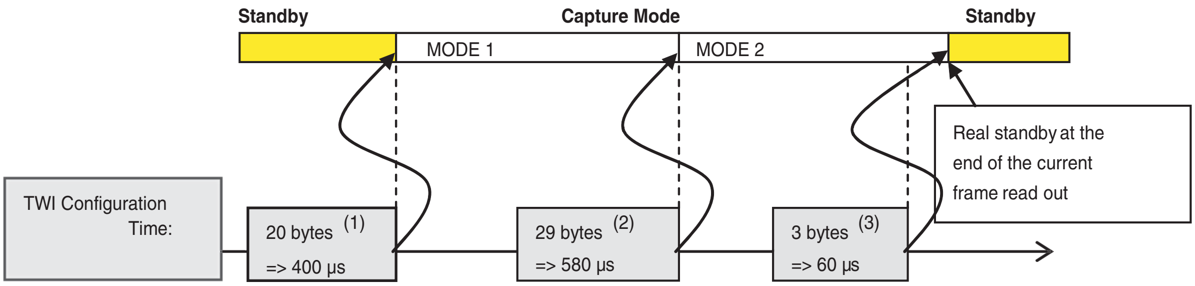
If the line length set is lower than the minimum line length required by the sensor it will not be taken into account.

9.9 Timing Modes

TWI registers are used to control the timing. For information on *integration time* by: frame_tint (see Section 10.4.2.1). For *waiting time* by: frame_twait (see Section 10.4.2.2).

Figure 9-4 is an example; the real configuration might be different

Figure 9-4. Example of Mode Changing



Inside the gray labels are the number of bytes sent to the sensor and the necessary time.

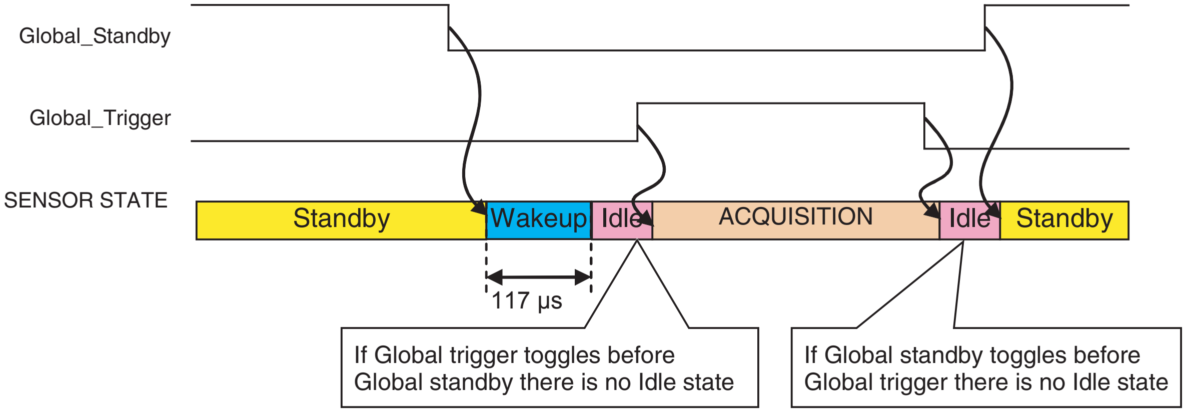
Notes:
1. During standby, configuration of the next acquisition, *frame_cfg_subsfactor, frame_tint*, gain, ROI … The wakeup request must be sent in the last byte.
2. Change of sensor configuration + communication of 10 filter parameters by TWI.
3. After standby request, standby is effective after the end of the current image (current image is finished after its “wait” phase in serial, and after its integration phase in overlap).

If no new parameter value is sent through TWI, the next frame is grabbed with all previous values (example: *frame_tint, frame_twait*, ROI parameters, etc.).

General comments on following timings:

- Gray dash areas in the two TWI lines ▨ mean:
  - The configuration sent inside this area will not be active until the next image
  - The configuration read inside this area is not valid
- Tint stands for integration time

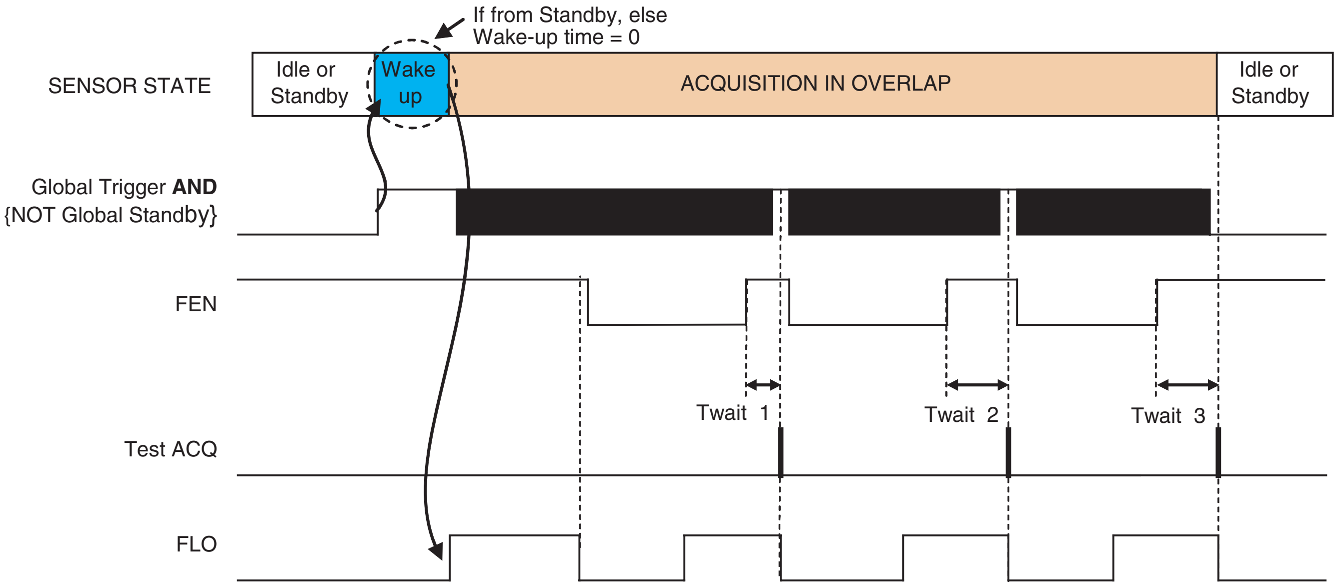
Figure 9-5. Overall State Timing Diagrams


Global_Standby
Global_Trigger
SENSOR STATE
Standby
Wakeup
Idle
ACQUISITION
Idle
Standby
117 µs
If Global trigger toggles before Global standby there is no Idle state
If Global standby toggles before Global trigger there is no Idle state

Notes:

- Global_Standby = [*pad_stdby_ena* **and** (*pad_stdby_inv* **xor** pin_stdby)] **or** *stdby_rqst*
- Global_Trigger = [*pad_trig_ena* **and** (*pad_ trig _inv* **xor** pin_trig)] **or** *trig*
- pin_stdby and pin_trig logical states come from STANDBY (pin 25) and TRIG (pin 24) pins
- *pad_stdby_ena, pad_stdby_inv, pad_trig_ena* and *pad_ trig _inv* bits come from pad_enable @hE TWI register see Section 10.4.1.7 "Standby and Trigger Configuration" on page 46.
- *stdby_rqst* and *trig* bits come from miscel_ctrl @hF TWI register see Section 10.4.1.8 "General Controls" on page 47.

Figure 9-6. Standby and Trigger Timing Diagrams in Overlap Mode

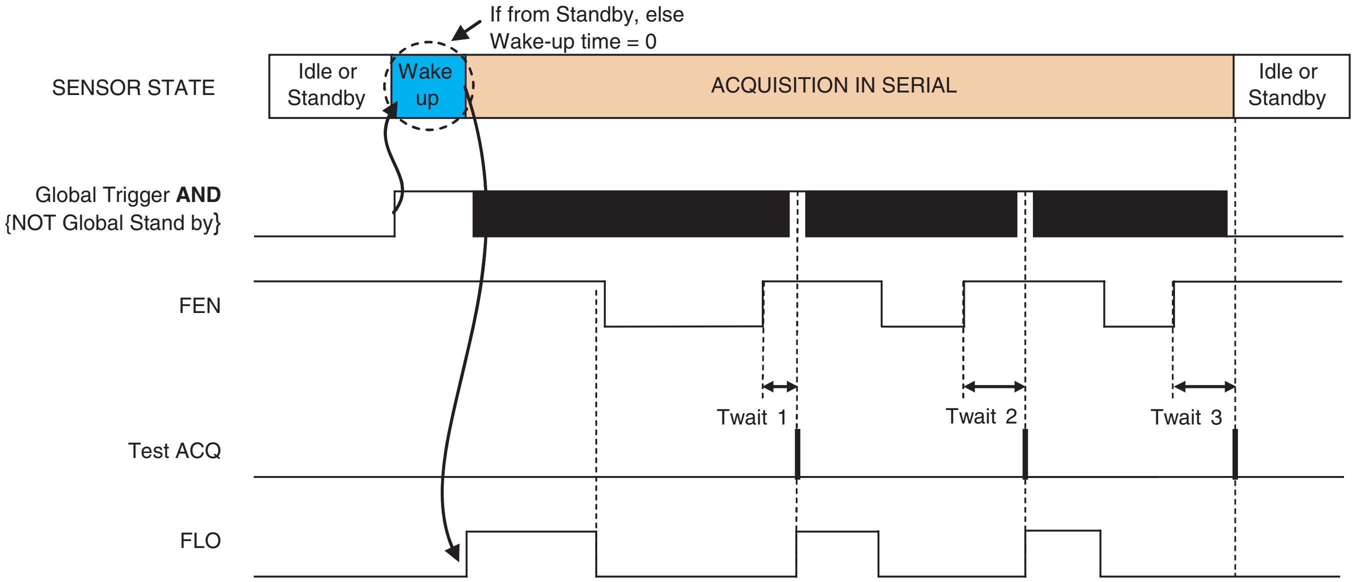


Notes:

- Test ACQ is the time when the Global Trigger and Global Standby states are tested by the internal logical.
- The last FLO pulse is not used.
- Twait = (*fb_frame_twait* + 4 + *bypass_f33*) * *Line_length* - 300 clk_pix.

See Section 10.4.1.8 "General Controls" on page 47 and Section 10.4.2.9 "Line Length" on page 56.

Figure 9-7. Standby and Trigger Timing Diagrams in Serial Mode



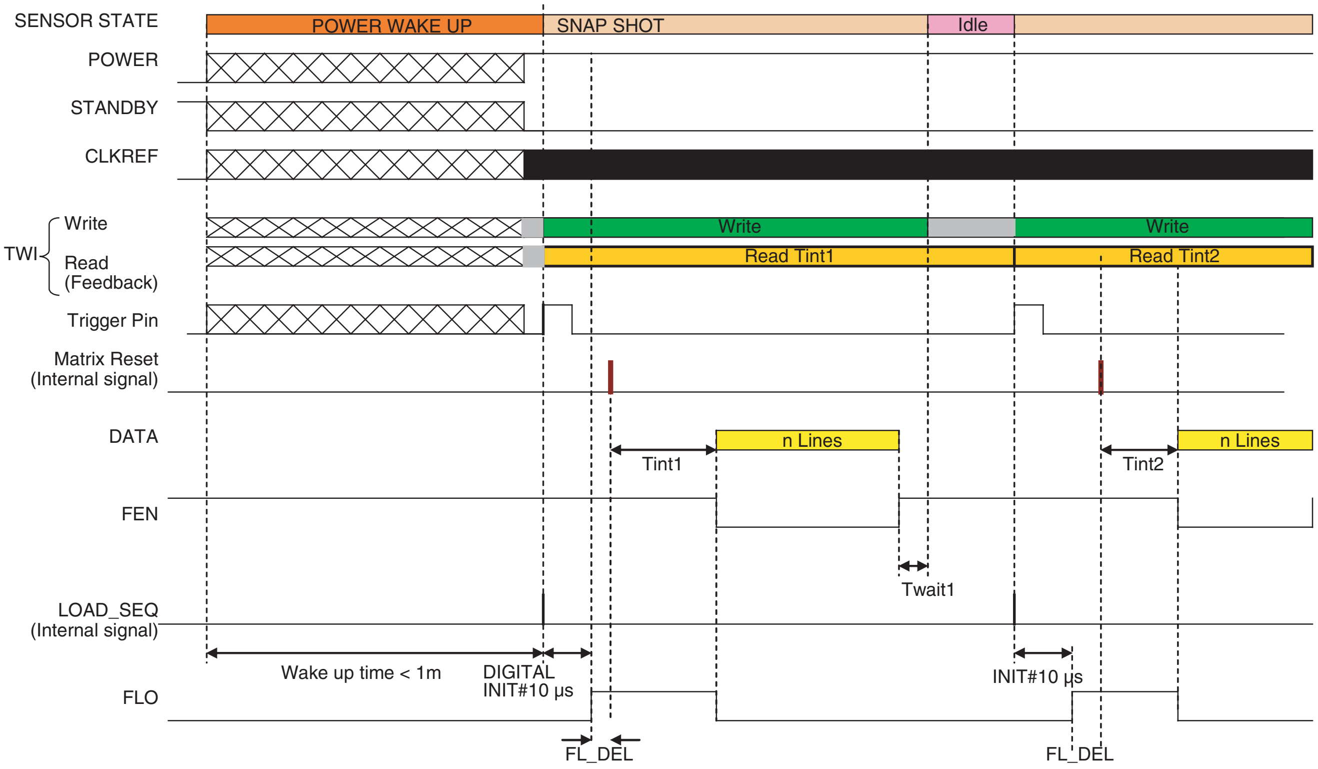
See Section 10.4.1.8 ”General Controls” on page 47 and Section 10.4.2.9 ”Line Length” on page 56.

Note: Twait = (*fb_frame_twait* + 4 + *bypass_f33*) * *Line_length* - 300 clk_pix

9.9.1 Image by Image Capture Controlled by Trigger

The following chronogram represents the *capture mode* started by a rising edge on the trigger pin.

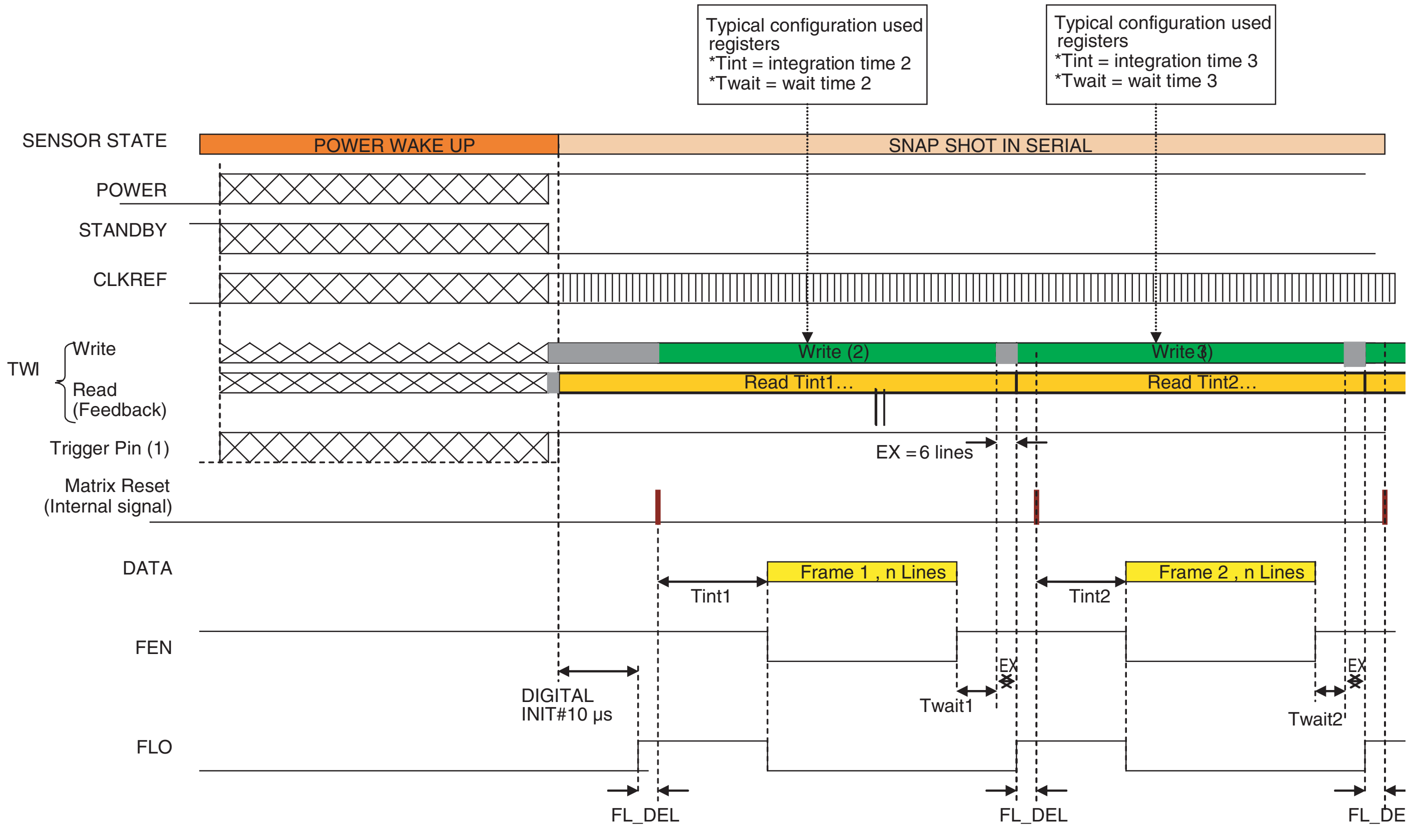
Figure 9-8. Capture Mode Timing



Note: Power is considered as ON when the power voltages have reached 90% of nominal value (3V and 1.65V).

9.9.2 Burst Image Capture in Serial Mode

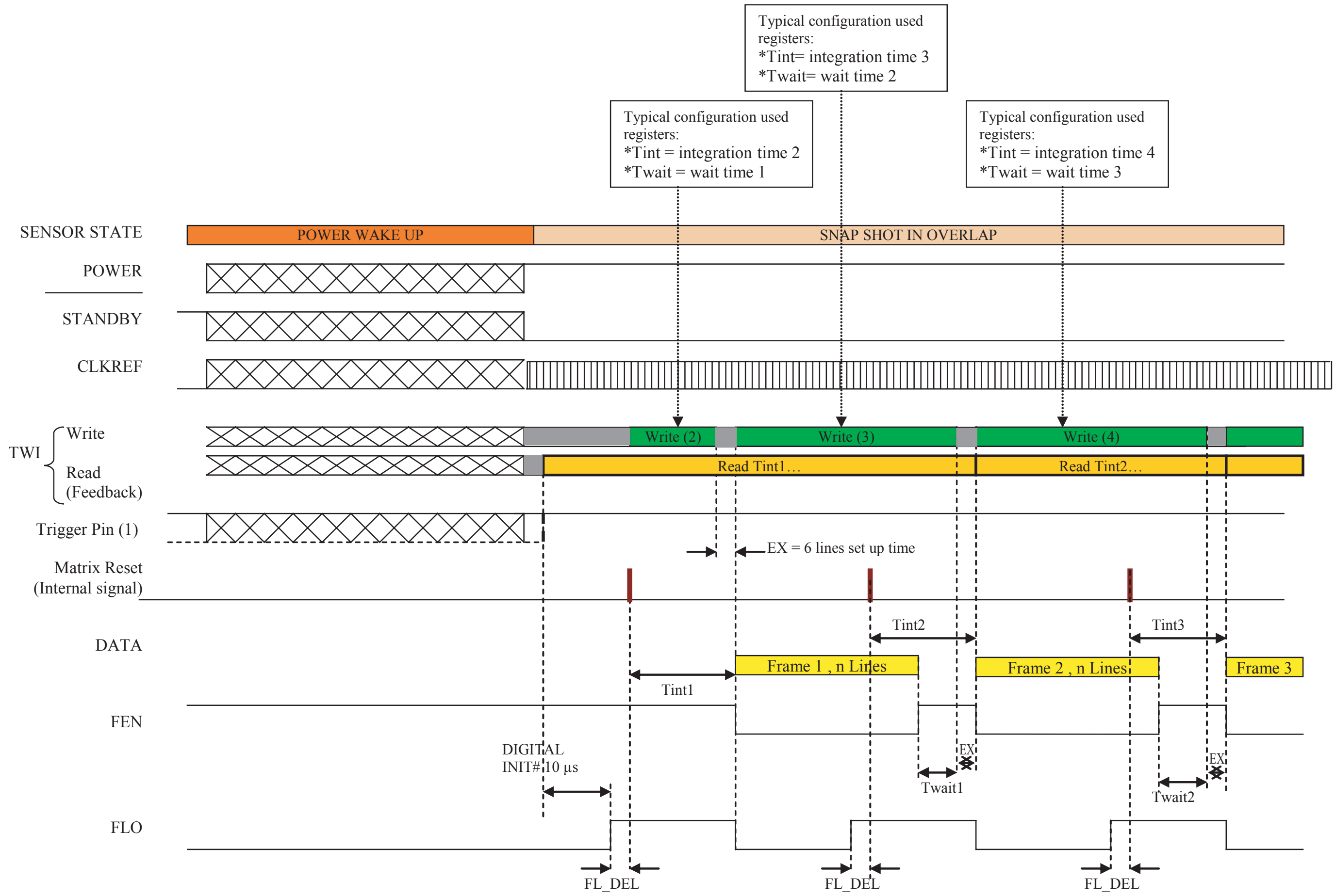
Figure 9-9. Serial Mode Timing



One image capture cycle is FL_DEL + Tint + Tread + Twait + EX.

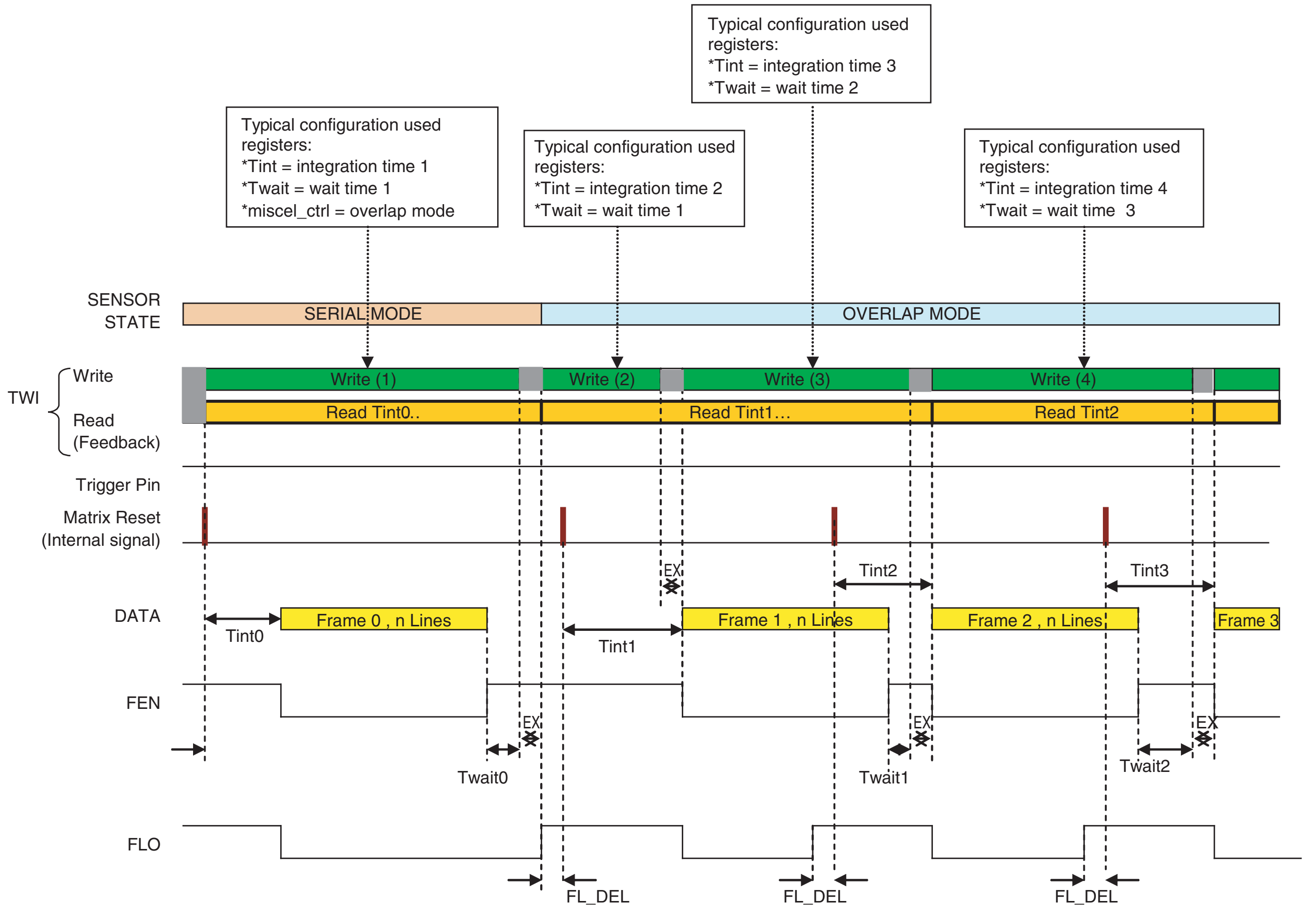
9.9.3 Burst Image Capture in Overlap Mode

Figure 9-10. Overlap Mode Timing



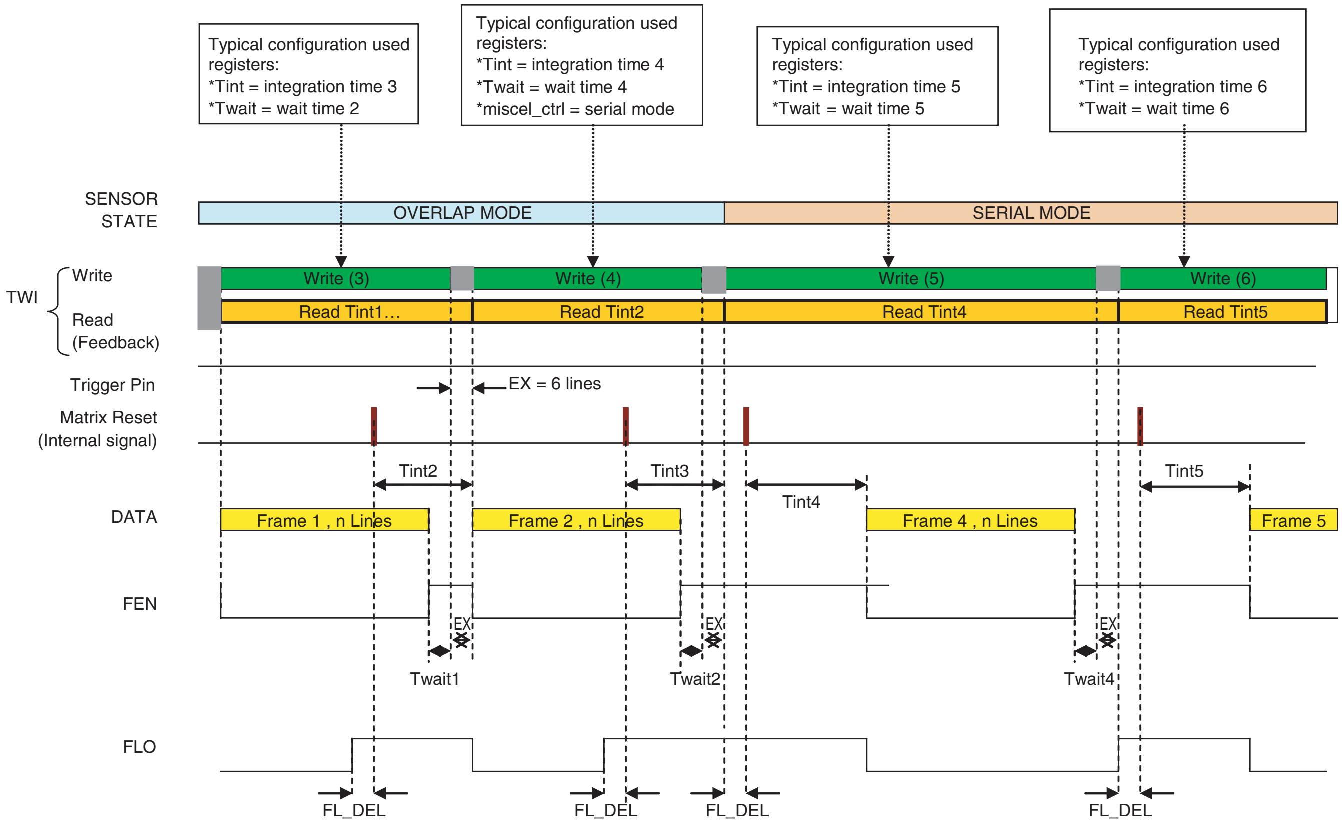
9.9.4 Serial Mode to Overlap Mode Transition

Figure 9-11. Serial Mode to Overlap Timing



9.9.5 Overlap Mode to Serial Mode Transition

Figure 9-12. Overlap to Serial Timing



Note: Frame 3 discarded means that the tint3 is never used, Frame 3 is discarded before it really exists. Tint3 has no influence if it is smaller than tread2+twait2. If it is greater, then you can send an abort to save valuable time.

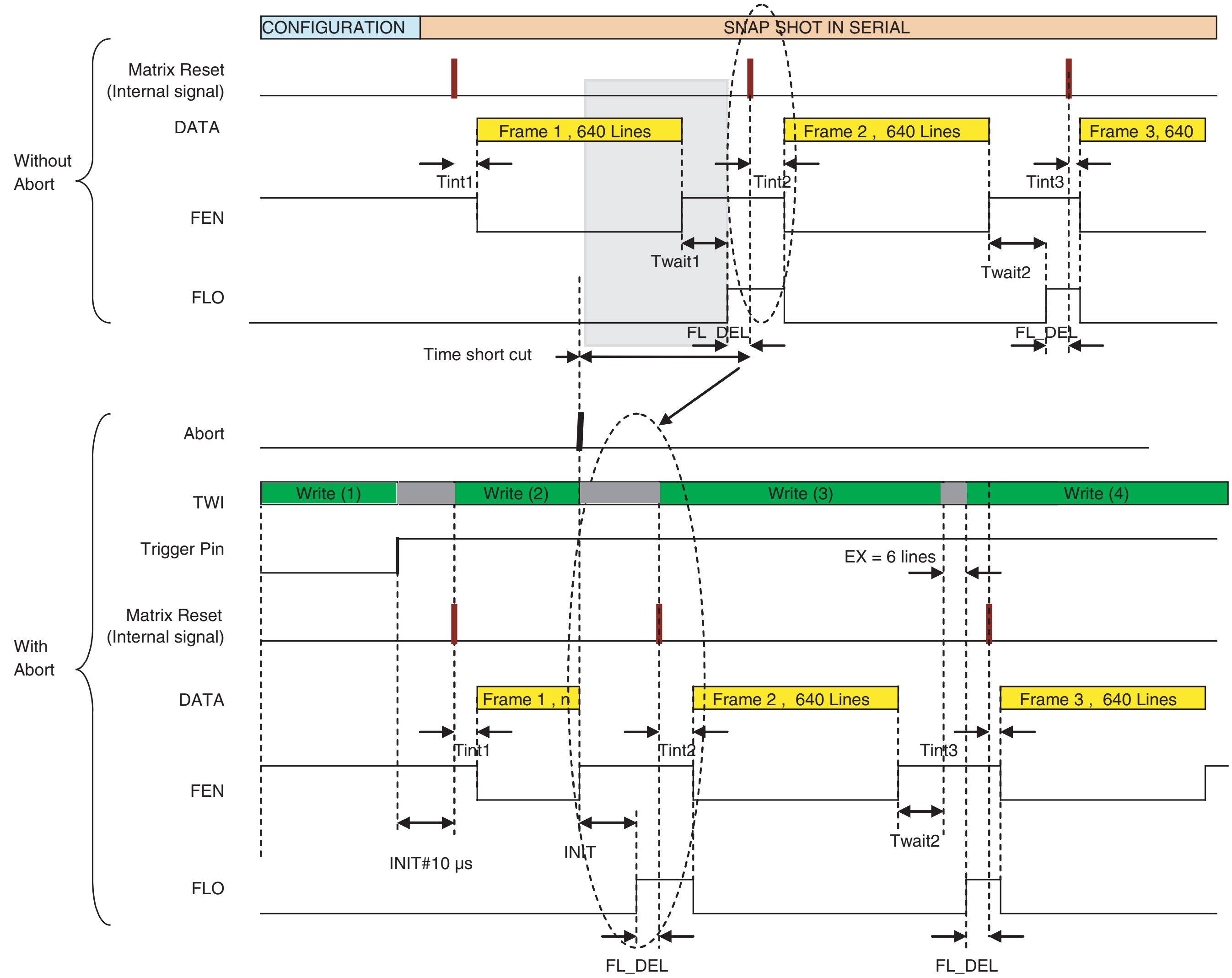
9.9.6 Abort Function

This function allows the application to abort the current image capture process. The data sent to the output bus is discarded.

After an abort process, the sensor behavior is as if the image had been read and the Twait was equal to zero. Figure 9-13 gives an example.

9.9.6.1 In Serial Mode

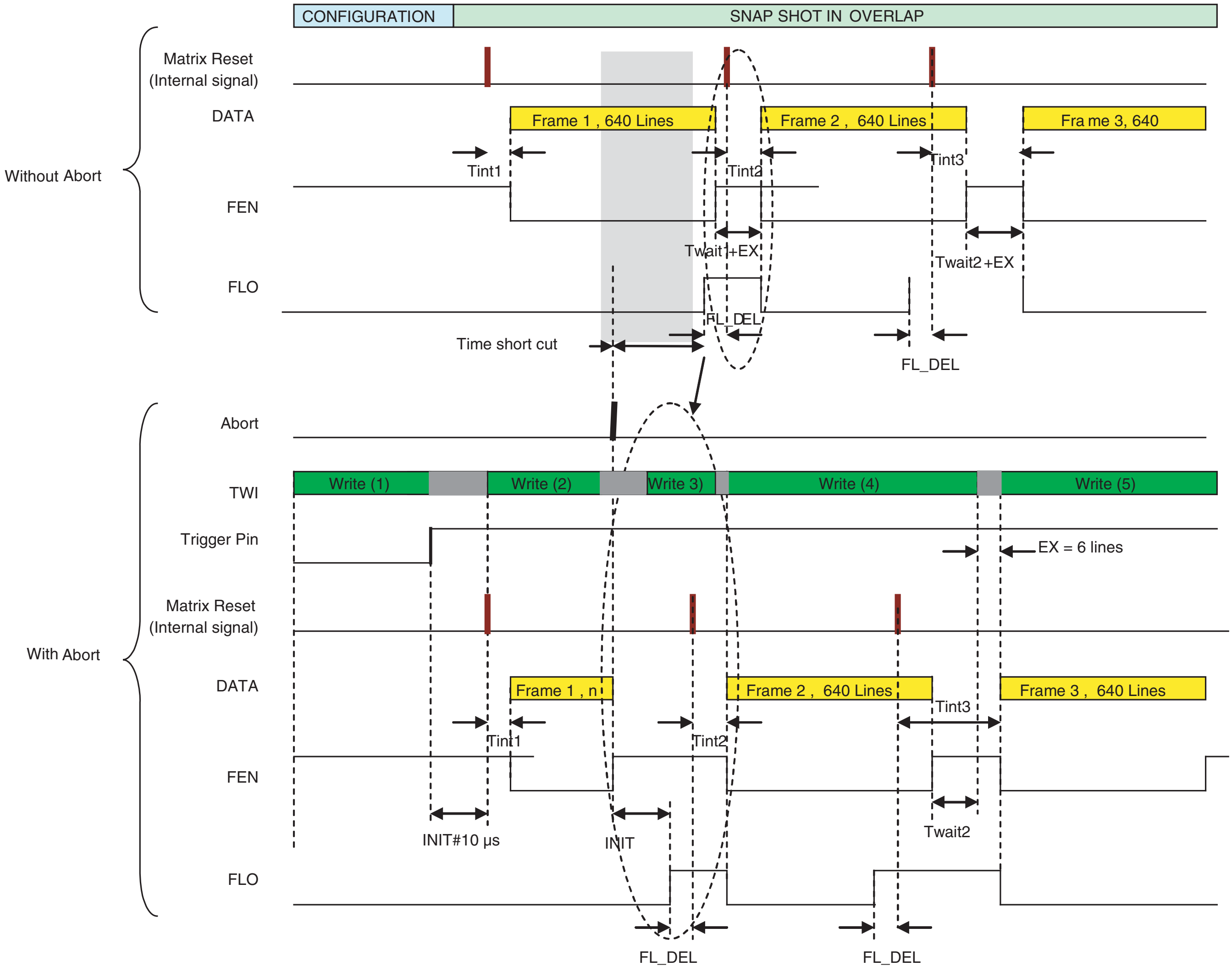
Figure 9-13. Abort Timing in Serial Mode



The reading process is finished at the end of the current line.

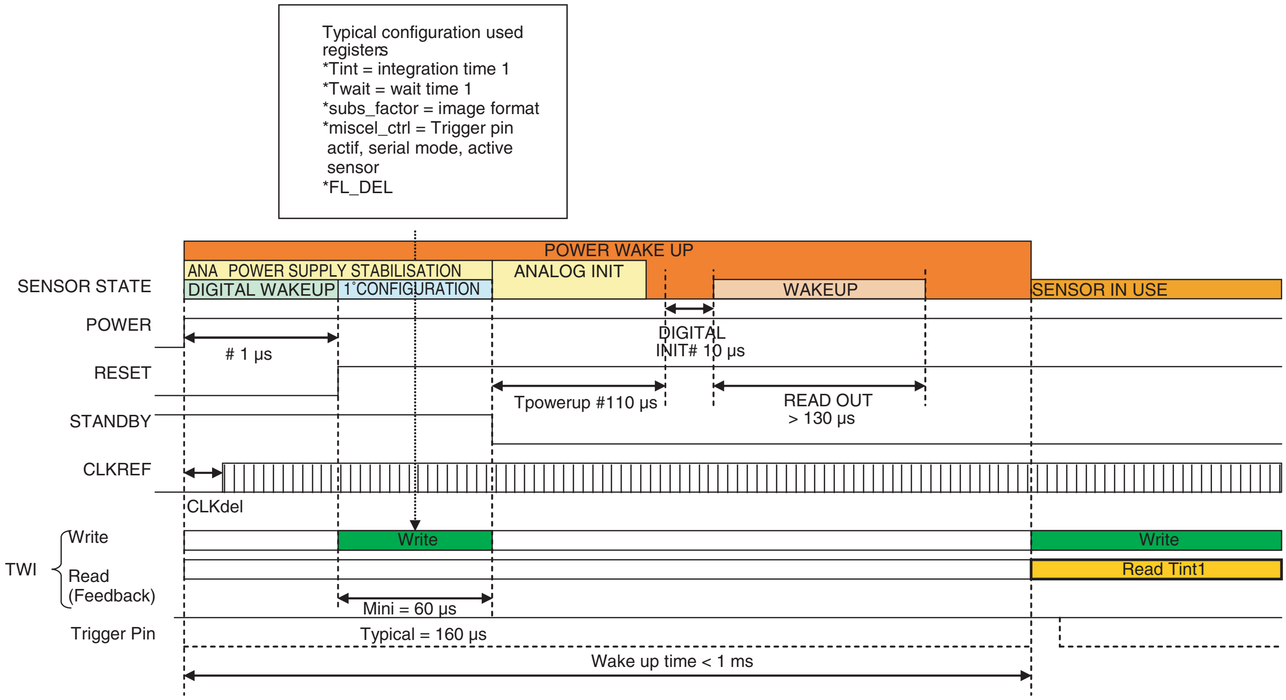
9.9.6.2 In Overlap Mode

Figure 9-14. Abort Timing in Overlap Mode



9.9.7 Power-up Sequence

Figure 9-15. Power-up Sequence



Notes:
1. First configuration duration depends on the number of TWI bytes to be set.
2. Wakeup sequence is programmable through TWI.
3. Analog power supply stabilized in the application.
4. Power up and power down sequences are indifferent
5. VDD18D must be on before using TWI as described in Figure 9-15.
6. VDD33A and VDD18A must be on before starting the first integration

9.10 Synchronization Pulse Timing

9.10.1 Data and Pixel Clock

Figure 9-16. Output Timing (Output load = 10 pF)

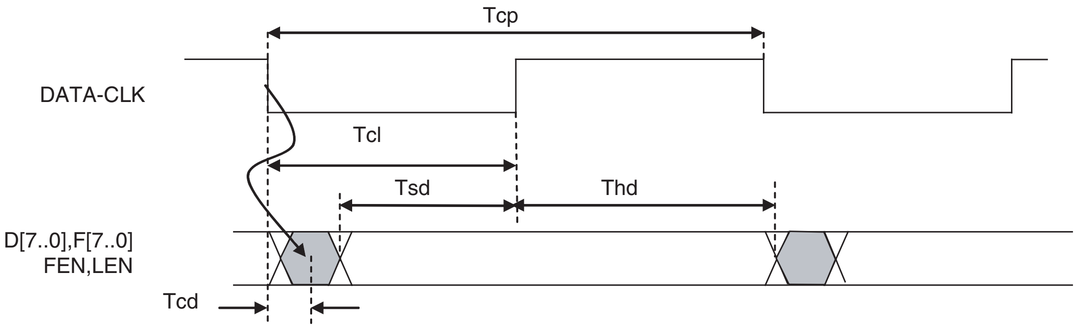


Table 9-1. Image Sensor Output Timing Specification

Parameter Definition	Symbol	Min	Typ	Max	Unit
Clock period	Tcp		20.8		ns
Clock low time[1]	Tcl	8	10.3	13	ns
Data setup time	Tsd	4			ns
Data hold Time	Thd	8			ns
Data_Clk to Data or FEN or LEN	Tcd	0		4	ns
Falling and rising edges on all signals with 10 pF load	Tr/Tf		2.2		ns

Note: 1. Including the clock input duty cycle and frequency precision.

9.10.2 Horizontal Timing

Figure 9-17. Horizontal Timings

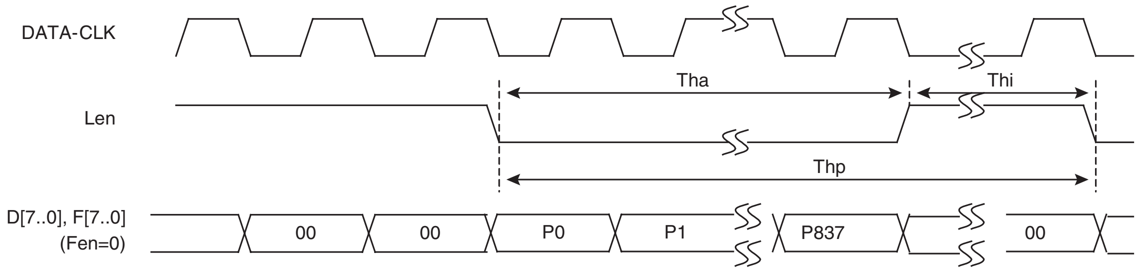


Table 9-2. Horizontal Timing Values

Parameter	Symbol	Default[2]	Unit
Horizontal active pixel[1]	Tha	838	DATA_CLK
Horizontal inactive pixel[1]	Thi	340	DATA_CLK
Horizontal period	Thp	1178	DATA_CLK

Notes: 1. Depends on ROI and subsampling.

2. These values are identical for clock divided by two or four.

9.10.3 Vertical Timing

Figure 9-18. Vertical Timings

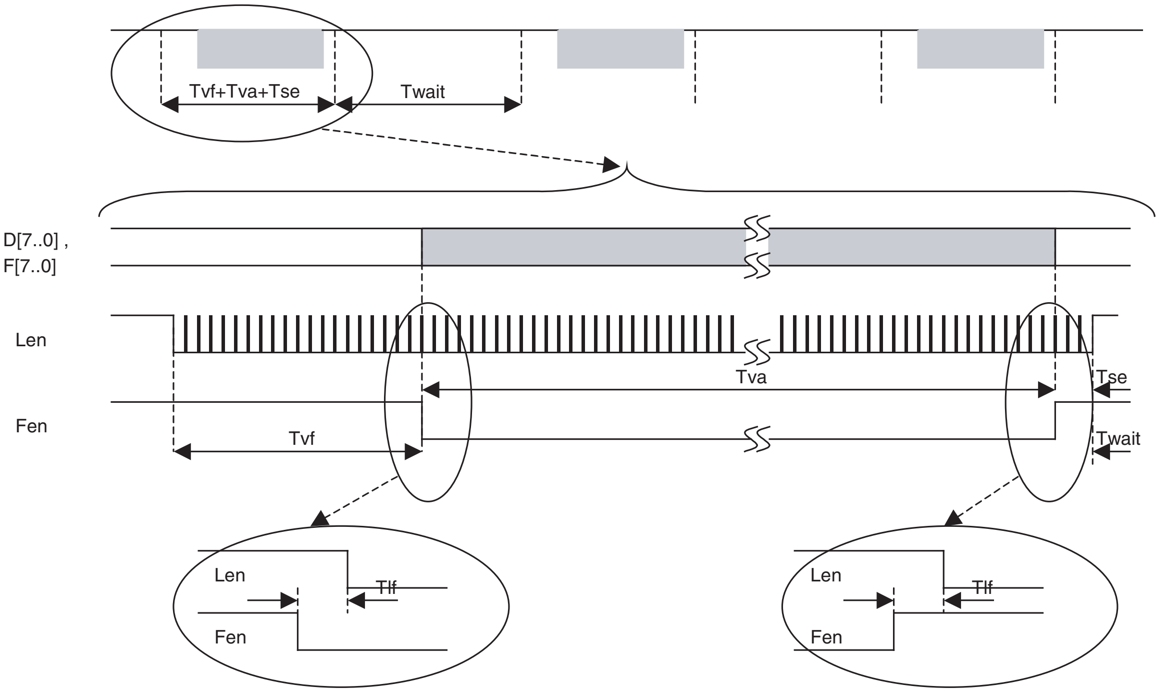


Table 9-3. Vertical Timing Values

Parameter	Symbol	3X3 Filter On	3X3 Filter Off	Unit
Vertical valid data[1]	Tva	640	640	Line period
First optical shielded line to vertical valid data	Tvf	12	11	Line period
Fen to synchro end	Tse	2	3	Line period
Fen to falling Len	Tlf	2	3	DATA_CLK

Note: 1. Depends on ROI and subsampling.

10. TWI

10.1 TWI Address

The address range is from h18 to h1B (expressed on 7 bits) and the two pins (see Section 15.1) define the 2 LSBs.

Address pins must be connected either to 0V (logical *0*) or to 1.8V (logical *1*). Therefore, first byte after the *start* procedure should be:

Table 10-1. TWI Address

MSB					A1	A0	LSB	Address
0	0	1	1	0	0	0	R/W	h18
0	0	1	1	0	0	1	R/W	h19
0	0	1	1	0	1	0	R/W	h1A
0	0	1	1	0	1	1	R/W	h1B

10.2 TWI Synchronization

There is no synchronization between the frame readout and the TWI registers writing and reading.

A *twi_lock* register can be used to enable writing of a coherent change made of several register writes (see Section 10.4.1.8).

it can be used as follows:

1. Lock the update of dynamic registers.
2. Make all required changes.
3. Unlock the update.

All the changes will be applied at once at the end of the same readout.

Reading or writing at the end of Twait during the 3 to 5 lines needed to update the dynamic registers might produce strange behavior or the sensor. It is recommended to not access to TWI during this period unlock mode period.

In case of overlap with tint > tread+twait, then the forbidden state is just before the end of tint. For security reasons in overlap, you should not access TWI from the end of twait to the beginning of next frame, etc.

10.3 Registers Overview

Description of all TWI registers of EV76C454 circuit. They are divided in two parts:

- 8-bit registers (address 0 to 127)
- 16-bit registers (address 128 to 255)

There are three types of registers:

- s: static
  - Read/Write registers
  - Value changes immediately upon write
  - These registers should be changed only during the standby mode
- d: dynamic
  - Read/Write registers
  - If *twi_lock*=0, value changes at end of current frame, (see Section 10.4.1.8).
  - If *twi_lock*=1, value is not updated into chip (but its kept in memory)
- f: feedback
  - Read-only registers
  - Values not available in idle mode, except for fb_status and mlbx_flag

Note that some specific bit of static registers acts like dynamic registers.

In the following tables, Fact = factory registers, only for optimization, no comment available in the document.

Table 10-2. *8-bit TWI Registers*

Adr (hx)	Register Name	Type	Bit	Content	See	
h0	*f33_config*	d	4	*f33_signed_filtout*	Section 10.4.1.1	Section 12.
			3-0	*f33_b_shift[3:0]*		
h1	*f33_coef_11*	d	7-0	*f33_coef_11[7:0]*	Section 10.4.1.2	
h2	*f33_coef_12*	d	7-0	*f33_coef_12[7:0]*		
h3	*f33_coef_13*	d	7-0	*f33_coef_13[7:0]*		
h4	*f33_coef_21*	d	7-0	*f33_coef_21[7:0]*		
h5	*f33_coef_22*	d	7-0	*f33_coef_22[7:0]*		
h6	*f33_coef_23*	d	7-0	*f33_coef_23[7:0]*		
h7	*f33_coef_31*	d	7-0	*f33_coef_31[7:0]*		
h8	*f33_coef_32*	d	7-0	*f33_coef_32[7:0]*		
h9	*f33_coef_33*	d	7-0	*f33_coef_33[7:0]*		
hA	*synchro*	s	7-6	*div_clk[1:0]*	Section 10.4.1.3	Section 11.1
			5	*dataclk_inv*		Section 9.2
			4	*sync_flash_inv*		
			3	*sync_fen_inv*		
			2	*sync_len_inv*		
			1	*mask_idle_data*		Section 9.3
			0	*mask_idle_len*		
hB	*frame_config*	d	4	*frame_cfg_flipv*	Section 10.4.1.4	Section 5.4
			3	*frame_cfg_fliph*		
			2-0	*frame_cfg_subsfactor[2:0]*		Section 5.5
hC	*frame_lin_log*	d	3-0	*frame_vlr_ctrl[3:0]*	Section 10.4.1.5	Section 5.6
hD	*frame_flash_config*	d	7	*flash_disa*	Section 10.4.1.6	Section 9.4
			6-0	*frame_flash_del[6:0]*		
hE	*pad_enable*	s	3	*pad_stdby_ena*	Section 10.4.1.7	Section 11.2.1
			2	*pad_stdby_inv*		
			1	*pad_trig_ena*		Section 9.5.1
			0	*pad_trig_inv*		
hF	*miscel_ctrl*	s	6	*output_hiz*	Section 10.4.1.8	Section 14.2.3
			5	*bypass_gco*		Section 12.4.1
			4	*bypass_f33*		Section 12.
			3	*twi_lock*		Section 10.2
			2	*overlap*		Section 9.6
			1	*trig*		Section 9.5.2
			0	*stdby_rqst*		Section 11.2

Table 10-2. *8-bit TWI Registers (Continued)*

h10	*mlbx_data*	s	1-0	*mlbx_abort_data[1:0]*	Section 10.4.1.9	Section 9.7
h11	*mlbx_flag_i*	f	1	*mlbx_fb_abort_clear*	Section 10.4.1.10	
			0	*mlbx_fb_abort_rqst*		
h12	*fb_state*	f	5	*fb_overflow*	Section 10.4.1.11	Section 10.6
			4	*fb_corrupted_frame*		
			3	*fb_idle_ack*		
			2	*fb_stdby_dig_ack*		
			1	*fb_stdby_itfr_ack*		
			0	*fb_stdby_ana_ack*		
h13	*pattern*	s	2	*pattern_ena*	Section 10.4.1.12	Section 8.
h40	*fa_carac_frame*	s			Fact	
h41	*fa_carac_analog*	s			Fact	
h42	*fa_reg_ana*	s			Fact	
h43	*fa_carac_chrono_and_clk*	s			Fact	
h44	*fa_low_pwr*	s			Fact	
h45	*fa_test*	s			Fact	
h46	*fa_carac_sdec_len*	s			Fact	
h47	*clamp_cfg*	s	4	*clamp_thld_lock[3:0]*	Section 10.4.1.13	Section 7.
			1	*clamp_locker_ena*		
			1	*clamp_defcor_disa*		
			1	*clamp_manual*		
h48	*clamp_v0_gain*	s	6	*clamp_v0_gain_correction[5:0]*	Section 10.4.1.14	
h49	*clamp_offset_diff_1*	s	7	*clamp_offset_diff_1[6:0]*	Section 10.4.1.15	
h4A	*pcl_offset_diff_2*	s	7	*clamp_offset_diff_2[6:0]*	Section 10.4.1.16	
h4B	*clamp_ana_offset*	s	8	*clamp_ana_offset[7:0]*	Section 10.4.1.17	
h4C	*clamp_dig_offset*	s	8	*clamp_dig_offset [7:0]*	Section 10.4.1.18	
h4D	*fb_clamp_ana_offset*	f	8	*fb_clamp_ana_offset*	Section 10.4.1.19	
h4E	*fb_clamp_dig_offset*	f	8	*fb_clamp_dig_offset[7:0]*	Section 10.4.1.20	
h4F	*fa_fb_test_bist_result*	f			Fact	
h50	*fa_fb_pwr_twakeup_itfr*	f			Fact	
h51	*fa_fb_frame_flash_del*	f			Fact	

Table 10-3. 16-bit Registers

Adr (hx)	Register Name	Type	Bit	Content	See	
h80	*frame_tint*	d	15-0	*frame_tint[15:0]*	Section 10.4.2.1	Section 9.9
h81	*frame_twait*	d	11-0	*frame_twait[11:0]*	Section 10.4.2.2	
h82	*frame_gain*	d	9-7	*frame_gain_analog[2:0]*	Section 10.4.2.3	Section 5.3
			6-0	*frame_gain_digital[6:0]*		
h83	*frame_roi_0c*	d	9-0	*frame_roi_0c[9:0]*	Section 10.4.2.4	
h84	*frame_roi_0l*	d	9-0	*frame_roi_0l[9:0]*	Section 10.4.2.5	
h85	*frame_roi_w*	d	9-0	*frame_roi_w[9:0]*	Section 10.4.2.6	
h86	*frame_roi_h*	d	9-0	*frame_roi_h[9:0]*	Section 10.4.2.7	
h87	*gco_val*	d	9-0	*gco_val[9:0]*	Section 10.4.2.8	Section 13.2
h88	*line_length_cfg*	d	11	*use_ext_line_length*	Section 10.4.2.9	Section 9.8
			10-0	*line_length[10:0]*		
h89	*fb_carac_line_length_seq*	f	10-0	*fb_line_length_seq[10:0]*	Section 10.4.2.10	Section 10.6
h8A	*fb_frame_tint_seq*	f	15-0	*fb_frame_tint_seq[15:0]*	Section 10.4.2.11	
h8B	*fb_frame_twait*	f	11-0	*fb_frame_twait[11:0]*	Section 10.4.2.12	
h8C	*fb_frame_roi_1c_seq*	f	9-0	*fb_frame_roi_1c_seq[9:0]*	Section 10.4.2.13	
h8D	*fb_frame_roi_1l_seq*	f	9-0	*fb_frame_roi_1l_seq[9:0]*	Section 10.4.2.14	
h8E	*fb_frame_roi_2c_seq*	f	9-0	*fb_frame_roi_2c_seq[9:0]*	Section 10.4.2.15	
h8F	*fb_frame_roi_2l_seq*	s	9-0	*fb_frame_roi_2l_seq[9:0]*	Section 10.4.2.16	
hC0	fa_pixtime_width	s			Fact	
hC1	fa_pixtime_tra_com	s			Fact	
hC2	fa_pixtime_sel	s			Fact	
hC3	fa_pixtime_res_com	s			Fact	
hC4	fa_pixtime_res_mem	s			Fact	
hC5	fa_pixtime_res	s			Fact	
hC6	fa_pixtime_shs	s			Fact	
hC7	fa_pixtime_shr1	s			Fact	
hC8	fa_pixtime_shr2	s			Fact	
hC9	fa_pixtime_enpix	s			Fact	
hCA	fa_pixtime_oc	s			Fact	

Table 10-3. 16-bit Registers (Continued)

Adr (hx)	Register Name	Type	Bit	Content	See
hCB	*fa_pixtime_res_on_tra_com*	s			Fact
hCC	*fa_pixtime_res_on_readout*	s			Fact
hCD	*fa_shield_cfg*	s			Fact
hCE	*fa_carac_ana*	s			Fact
hCF	*fa_twakeup*	s			Fact
hD0	*fa_debbug_0*	s			Fact
hD1	*fa_debbug_1*	s			Fact
hD2	*fa_debbug_2*	s			Fact
hD3	*fa_debbug_3*	s			Fact
hD4	*fa_debbug_4*	s			Fact
hD5	*fa_debbug_5*	s			Fact
hD6	*fa_debbug_6*	s			Fact
hD7	*fa_debbug_7*	s			Fact
hD8	*fa_debbug_8*	s			Fact
hD9	*fa_debbug_9*	s			Fact
hDA	*fa_debbug_A*	s			Fact
hDB	*fa_debbug_B*	s			Fact
hDC	*fa_carac_ana_force*	s			Fact
hDD	*fa_carac_ana_val*	s			Fact
hDE	*fa_carac_ana_gray_cnt*	s			Fact
hDF	*fa_carac_ana_alin*	s			Fact
hE0	*fa_carac_ana_acol*	f			Fact
hE1	*fa_fb_frame_lreadout_seq*	f			Fact
hE2	*fa_fb_frame_treadout_seq*	f			Fact
hFF	*fb_chip_id*	f	15-0	15-0fb_chip_id [15:0]	Section 10.4.2.17

10.4 Detailed Description

10.4.1 8-bit Customer Registers

*10.4.1.1 3 **X** 3 Filter Configuration*

Name	*f33_config*
Address	`h00`
Type	Dynamic
Default	h07

Default Value	Name	Description
`---0 ----`	*f33_signed_filtout*	filter output: **0 ➔Unsigned** 1 ➔Signed
`---- 0111`	*f33_b_shift[3:0]*	B filter factor value: (it is a shifting coefficient) Min: 0 Max: d12

*10.4.1.2 3 **X** 3 Filter Coefficient Values*

Name	*f33_coef_ij*
Address	`h01 to h09`
Type	Dynamic
Default	see table

Default Value	Name	Description
`See below`	*f33_coef_ij[7:0]*	9 filter factor values (signed) Min: –128 (10000000) Max: +127 (01111111)

Address	h01	h02	h03
Coefficient	$C_{-1,-1}$	$C_{0,-1}$	$C_{1,-1}$
Default Value	h01	h0B	h01
Address	h04	h05	h06
Coefficient	$C_{-1,0}$	$C_{0,0}$	$C_{1,0}$
Default Value	h0B	h4F	h0B
Address	h07	h08	h09
Coefficient	$C_{-1,1}$	$C_{0,1}$	$C_{1,1}$
Default Value	h01	h0B	h01

10.4.1.3 Synchronization Configuration

Name	*Synchro*
Address	h0A
Type	Static
Default	h22

Default Value	**Name**	**Description**
00-- ----	*div_clk[1:0]*	Master clock divider: **00➔ Not divided** 01➔ Divided by 2 10➔ Divided by 4 11➔ Divided by 4
--1- ----	*dataclk_inv*	Data clock polarity: (see Section 9.10.1) 0 ➔Data_are output on Data_CLK rising edge **1 ➔ Data_are output on Data_CLK falling edge**
---0 ----	*sync_flash_inv*	Flash polarity: **0 ➔ FLO output is active high** 1 ➔ FLO output is active low
---- 0---	*sync_fen_inv*	Frame Enable polarity: **0 ➔FEN is active low (0 during active part of line)** 1 ➔ FEN is active high (1 during active part of line)
---- -0--	*sync_len_inv*	Line Enable polarity: **0 ➔ LEN is active low (0 during active part of line)** 1 ➔ LEN is active high (1 during active part of line)
---- --1-	*mask_idle_data*	Data activity when FEN or LEN are inactive: **1 ➔ No activity: Data outputs all forced at 0 when outside active part of line or outside active part of image** 0 ➔ Do not care
---- ---0	*mask_idle_len*	LEN activity when FEN is inactive **0 ➔ passes all calculated "LEN"** 1 ➔masks LEN output with high level (outside active image)

10.4.1.4 Readout Configuration

Name	*frame_config*
Address	`h0B`
Type	Dynamic
Default	h00

Default Value	Name	Description
`---0 ----`	*frame_cfg_flipv*	**0→No vertical flip** 1→Vertical flip is enabled (lines are read in decreasing order)
`---- 0---`	*frame_cfg_fliph*	**0→No horizontal flip** 1→Horizontal flip is enabled (columns are read in decreasing order)
`---- -000`	*frame_cfg_subsfactor[2:0]*	Subsample factor = $2^{subsample}$ **000 min value:1** 100 max value: 16

For flip matter, (see Section 5.4.1).

10.4.1.5 Linear or Logarithmic Configuration

Name	*frame_line_log*
Address	`h0C`
Type	Dynamic
Default	h01

Default Value	Name	Description	
`---- 0001`	*frame_vlr_ctrl[3:0]*	Control for lin/log part: 0000 Do not used **Min: 0001 linear mode 0.225V** Max: 1110 maximum log mode 1111 External VLR	VLR = Frame_line_log × 0.075 + 0.225V

10.4.1.6 Flash Configuration

Name	*frame_flash_config*
Address	h0D
Type	Dynamic
Default	h3D

Default Value	Name	Description
`0--- ----`	flash_disa	FLash Output (FLO) 1➔Disable **0➔Enable**
`-011 1101`	*frame_flash_del[6:0]*	Delay from start of FLO to start of integration Step= (800 × Master clock) ≈ 16.7 µs @ 48 MHz if div_clk=00 Min h00 = 0 ms (flash starts with integration) Max h7F (d127) ≈ 2 ms It is better to keep: -the LSB at 0 when using the div_clk=01 (Master clock divided by two) -the 2 LSB at 0 when using div_clk=10 or 11 (Master clock divided by four)

10.4.1.7 Standby and Trigger Configuration

Name	*pad_enable*
Address	h0E
Type	Static
Default	h0A

Default Value	Name	Description
`---- 1---`	*pad_stdby_ena*	1➔**Enable use of standby input pad**
`---- -0--`	*pad_stdby_inv*	**0➔*Standby* input is active high (when requested)** 1➔*Standby* input is active low (when requested)
`---- --1-`	*pad_trig_ena*	**1➔Enable use of TRIG input pad**
`---- ---0`	*pad_trig_inv*	**0➔TRIG input is active high (when enabled)** 1➔TRIG input is active low (when enabled)

10.4.1.8 General Controls

Name	*miscel_ctrl*
Address	h0F
Type	Static
Default	h67

Default Value	**Name**	**Description**
-1-- ----	*output_hiz*	**1➔ Forces all output pads to high impedance** 0➔ No effect
--1- ----	*bypass_gco*	Gamma correction activity: 0➔Gamma correction is applied on D[7:0] output **1➔Gamma correction is bypassed**
---0 ----	*bypass_f33*	3x3 filter activity: **0➔Filter is activated and its result is available on FIL pads** 1➔Filter is bypassed and FIL[7:0] pads are set to 0
---- 0---	*twi_lock*	**0➔Dynamic TWI registers are updated at end of frame** 1➔Dynamic TWI registers are not updated into chip (locked)
---- -1--	*overlap*	Readout mode: 0➔Serial mode **1➔Overlap mode** **This bit is a dynamic bit**
---- --1-	*trig*	0➔ No action **1➔ Same effect as active TRIG input: launches an acquisition, and keep acquiring while 1.** There is no auto-reset on this bit; to clear it, one needs to set it to 0.
---- ---1	*stdby_rqst*	Standby request: 0➔ Normal operation **1➔ Standby requested: finish current image and switch to standby mode**

Note on trig:

pad_trig_ena and pad_trig_inv have no influence on action of this twi trig bit.

To send a TRIG to chip, you have to send:

- Either an active TRIG_from_pad
- Or an active TRIG_from_twi

Note on stdby_rqst:

pad_stdby_rqst_ena and pad_stdby_rqst_inv have no influence on action of this stdby_rqst bit

To send a STDBY_RQST to chip, you have to send

- Either an active STDBY_RQST_from_pad,
- Or an active STDBY_RQST_from_twi

10.4.1.9 Mailbox ABORT Trigger

Name	*mlbx_data*
Address	`h10`
Type	Static
Default	h00

Default Value	Name	Description
`---- --00`	*mlbx_abort_data[1:0]*	When written (to any value), triggers the ABORT process and sets the mailbox flag high

10.4.1.10 Mailbox ABORT Flag

Name	*mlbx_flag_i*
Address	`h11`
Type	Feedback

Active Bits	Name	Description
`---- --X-`	*mlbx_fb_abort_rqst*	Internal: 0➔No abort is requested 1➔An abort was requested, and is being treated. It will be granted when this bit will go back to 0
`---- ---X`	*mlbx_fb_abort_clear*	Internal: A pulse sent internally clears the mailbox when the ABORT is finished 0➔No action 1➔ Clearing the flag

Note: When an abort is requested, it is granted in less than one line; it means less than 24 µs. Since a TWI access lasts at least 60 µs, it should never be possible to read the mlbx_fb_abort_rqst feedback at *1.*

10.4.1.11 *Overall Status*

Name	*fb_state*
Address	`h12`
Type	Feedback

Active Bits	Name	Description
`--X- ----`	*fb_overflow*	When high, means that an overflow was issued in the process because of bad tint/twait/flash_del/line_length prog
`---X ----`	*fb_corrupted_frame*	When high, means that the frame is corrupted because of a bad ROI programming (too big)
`---- X---`	*fb_idle_ack*	When high, means that the chip is in *idle mode*
`---- -X--`	*fb_stdby_dig_ack*	When high, means that *digital* part is in *standby* mode
`---- --X-`	*fb_stdby_itfr_ack*	When high, means that *analog* part is in *interframe standby* mode (analog partially off)
`---- ---X`	*fb_stdby_ana_ack*	When high, means that *analog* part is in *standby* mode

10.4.1.12 *Pattern Generator*

Name	*ena_test_pattern*
Address	`h13`
Type	Static
Default	h00

Default Value	Name	Description
`---- --00`	*ena_test_pattern[1:0]*	**00➔No test pattern: video is output** 01➔Moving test pattern 10➔Fixed test pattern 11➔Functional test pattern

10.4.1.13 Clamp Configuration

Name	*clamp_cfg*
Address	h47
Type	Static
Default	h15

Default Value	Name	Description
---- 0101	*clamp_thld_lock[3:0]*	Represents the threshold offset value, from which the clamp offset is re-applied to the picture
---1 ----	*clamp_locker_ena*	**1➔ Enables the lock of the clamp** *0*➔ Disables the lock of the clamp
--0- ----	*clamp_defcor_disa*	**0➔ Enables the default correction** 1➔ Disables the default correction
-0-- ----	*clamp_manual*	**0➔ Automatic clamp** 1➔ Puts the clamp in manual mode

10.4.1.14 Clamp V0 Gain Correction

Name	*clamp_v0_gain_correction*
Address	h48
Type	static
Default	h00

Default Value	Name	Description
--00 0000	*clamp_v0_gain_correction[5:0]*	Gain correction applied to the offset

10.4.1.15 Clamp Manual Offset In Automatic Mode

Name	*clamp_offset_diff_1*
Address	h49
Type	Static
Default	h00

Default Value	Name	Description
-000 0000	*clamp_offset_diff_2[6:0]*	Manual offset value when the clamp is in automatic mode

10.4.1.16 Post Clamp Manual Offset

Name	*pcl_offset_diff_2*
Address	h4A
Type	Static
Default	h00

Default Value	Name	Description
-000 0000	*clamp_offset_diff_2[6:0]*	Manual post-clamp offset value in automatic mode

10.4.1.17 Clamp Analog Offset in Manual Mode

Name	*clamp_ana_offset*
Address	h4B
Type	Static
Default	h00

Default Value	Name	description
0000 0000	*clamp_ana_offset[7:0]*	Digital offset value applied to the offset in <u>manual</u> mode. **This value must not exceed hA1.**

10.4.1.18 Clamp Digital Offset in Manual Mode

Name	*clamp_dig_offset*
Address	h4C
Type	Static
Default	h00

Default Value	Name	Description
0000 0000	*clamp_dig_offset [7:0]*	Digital offset value applied to the offset in <u>manual</u> mode

10.4.1.19 Clamp's Analog Offset

Name	*fb_clamp_ana_offset*
Address	h4D
Type	Feedback

Active Bits	Name	description
XXXX XXXX	*fb_clamp_ana_offset[7:0]*	Analog offset calculated internally by the clamp

10.4.1.20 Clamp's Digital Offset

Name	*fb_clamp_dig_offset*
Address	h4E
Type	Feedback

Active Bits	Name	Description
XXXX XXXX	*fb_clamp_dig_offset[7:0]*	Digital offset calculated internally by the clamp

If this feedback is different from 0 that means that the output will never reach the 255 saturation.

10.4.2 16-bit Customer Registers

10.4.2.1 Integration Time

Name	*frame_tint*
Address	h80
Type	Dynamic
Default	h012C

Default Value		Name	Description
0000 0001	0010 1100	*frame_tint*	Integration duration adjustment. Software step = (800 x Master clock) ≈ 16.7 µs @ 48 MHz if div_clk=00 Real duration: The integration time is rounded at the nearest number of lines above the programmed time. Min: h0000 ≈ 1 line of integration, ≈ 24.5 µs @ 48 MHz if div_clk=00 Max: hFFFF ≈ 1.09 s It is better to keep: -the LSB at 0 when using the div_clk=01(Master clock divided by 2) -the 2 LSB at 0 when using div_clk=10 or 11 (Master clock divided by 4)

10.4.2.2 Waiting Time

Name	*frame_twait*
Address	h81
Type	Dynamic
Default	h000

Default Value		Name	Description
---- 0000	0000 0000	*frame_twait*	Wait duration between two frames. It specifies the max time for twi communication after end of frame, to program next acquisition parameters. step= (800 × master clock) ≈ 16.7 µs **Min: h000 → no time after end of frame** Max: hFFF→ 68.2 ms It is better to keep: -the LSB at 0 when using the div_clk=01 (Master clock divided by 2) -the 2 LSB at 0 when using div_clk=10 or 11 (Master clock divided by four)

10.4.2.3 Analog and Digital Gain

Name	*frame_gain*
Address	h82
Type	Dynamic
Default	h000

Default Value		Name	Description
---- --00	0--- ----	*frame_gain_analog*	Analog gain applied (see Table 10-4) **Min 000→ 1** Max 111→ 8
---- ----	-000 0000	*frame_gain_digital*	digital gain, applied after the offset substraction digital gain = 1 + dig_gain / 32 **Min 0000000→ digital gain = 1** Max 1111111→digital gain = 4.97

Table 10-4. Analog and Digital Gains

Global Gain	Analog Gain		Digital gain
	G<2:0> code	Gain Value	
[1 to 1.5 [	000	1	1 to 1+ 15/32 (1.47…)
[1.5 to 2 [	001	1.5	1 to 1+ 10/32 (1.31…)
[2 to 3 [	010	2	1 to 1+ 15/32 (1.47…)
[3 to 4 [	011	3	1 to 1+ 10/32 (1.31…)
[4 to 6 [	100	4	1 to 1+ 15/32 (1.47…)
[6 to 7.875]	101	6	1 to 1+ 10/32 (1.31…)
[8 to 39.75]	110 and 111	8	1 to 1+ 127/32 (4.97…)

10.4.2.4 ROI First Column

Name	*frame_roi_0c*
Address	h83
Type	Dynamic
Default	h006

Default Value		Name	Description
---- --00	0000 0110	*frame_roi_0c*	Address in pixel of the first column read for the ROI definition **Min→ 0** Max→ d875

10.4.2.5 ROI First Line

Name	*frame_roi_0l*
Address	h84
Type	Dynamic
Default	h006

Default Value		Name	Description
---- --00	0000 0110	*frame_roi_0l*	Address in pixel of the first line read for the ROI definition **Min→0** Max→d651

10.4.2.6 ROI Width

Name	*frame_roi_w*
Address	h85
Type	Dynamic
Default	h360 (d864)

Default Value		Name	Description
---- --11	0110 0000	*frame_roi_w*	Width of the ROI in pixel Min➔d16 Max➔d876

10.4.2.7 ROI Height

Name	*frame_roi_h*
Address	h86
Type	Dynamic
Default	h280 (d640)

Default Value		Name	Description
---- --10	1000 0000	frame_roi_h	Height of the ROI in pixel Min➔d16 Max➔d652

10.4.2.8 Gamma Correction Factor

Name	*gco_val*
Address	h87
Type	Static
Default	h0100

Default Value		Name	Description
---- --01	0000 0000	*gco_val*	Value applied for Gamma correction: γ = 256/decimal value Min➔ d64 means γ = 4 **h0100 means** γ = 1 Max➔ d1023 means γ = 1/4

10.4.2.9 *Line Length*

Name	*line_length_cfg*
Address	`h88`
Type	Dynamic
Default	h49A

Default Value		Name	Description
`---- 0---`	`---- ----`	*use_ ext_line_length*	**0➔The line length is automatically calculated** 1➔The line length is given as a TWI parameter (line_length)
`---- -100`	`1001 1010`		Length of one line in Data Clock, used if *use_ext_line_length* is set to 1. The default value is d1178 and corresponds to the minimum line length allowed and used if this value is set at a lower value.

10.4.2.10 *Line Length Feedback*

Name	*fb_carac_line_length_seq*
Address	`h89`
Type	Feedback

Active Bits		Name	Description
`---- -XXX`	`XXXX XXXX`	fb_line_length_seq	The line length as calculated internally

10.4.2.11 *Integration Time Feedback*

Name	*fb_frame_tint_seq*
Address	`h8A`
Type	Feedback

Active Bits		Name	Description
`XXXX XXXX`	`XXXX XXXX`	*fb_frame_tint_seq*	The integration time as calculated internally in number of lines

10.4.2.12 *Waiting Time Feedback*

Name	*fb_frame_twait*
Address	`h8B`
Type	Feedback

Active Bits		**Name**	**Description**
`---- XXXX`	`XXXX XXXX`	*fb_frame_twait*	The wait time as calculated internally in number of lines fb_frame_twait **= FLOOR [frame_twait x 800 / fb_carac_line_length_seq]** Where FLOOR means "rounded to the next lower integer."

10.4.2.13 *First Column of Effective ROI Coordinates Feedback*

Name	*fb_frame_roi_1c _seq*
Address	`h8C`
Type	Feedback

Active Bits		**Name**	**Description**
`---- --XX`	`XXXX XXXX`	*fb_frame_roi_1c _seq*	Absolute address of effective ROI's first column, as calculated internally

10.4.2.14 *First Line of Effective ROI Coordinates Feedback*

Name	*fb_frame_roi_1l_seq*
Address	`h8D`
Type	Feedback

Active Bits		**Name**	**Description**
`---- --XX`	`XXXX XXXX`	*fb_frame_roi_1l_seq*	Absolute address of effective ROI's first line, as calculated internally

10.4.2.15 *Last Column of Effective ROI Coordinates Feedback*

Name	*fb_frame_roi_2c_seq*
Address	`h8E`
Type	Feedback

Active Bits		**Name**	**Description**
`---- --XX`	`XXXX XXXX`	fb_frame_roi_2c_seq	Absolute address of effective ROI's last column, as calculated internally

10.4.2.16 Last line of Effective ROI Coordinates Feedback

Name	f*b_frame_roi_2l_seq*
Address	`h8F`
Type	Feedback

Active Bits		**Name**	**Description**
`---- --XX`	`XXXX XXXX`	*fb_frame_roi_2l_seq*	Absolute address of effective ROI's last line, as calculated internally

10.4.2.17 fb_chip_id - Chip Identification Register

Name	*fb_chip_id*
Address	`hFF`
Type	Feedback

Active Bits		**Name**	**Description**
`0000 0111`	`0000 0001`	*fb_chip_id*	Gives the ID of the chip: here it is 0x0701. It is fixed

10.5 TWI Description

The TWI-bus is a two wires half-duplex link used to write to and to read from the sensor's internal configuration registers.

As the TWI clock SCL is an input pin, the device never controls the SCL line (slave type device). Data is transferred into and out of the sensor through the bidirectional pin SDA.

SCL and SDA are open drain. They require an off-chip pull-up resistor to VDD18D; *the pull-up resistor might be tied to 3.3V but the sensor will not respect the VIL of I^{2}C standard*. The resistors value should be computed according to I^{2}C standard. SDA can be pulled down either by the master or by one of the other slave devices connected to the serial bus. The TWI protocol determines at any time which one is allowed to pull the SDA line low.

To initiate a transmission, the master sends a start bit followed by the slave device address: In the following text, as example, h12.

Only the slave device which has identified this address is able to process data on SDA line, until the master terminates the transmission by emitting a stop bit. Others slaves stay in idle state and drive SDA high during this period.

The addressed slave acknowledges each received byte. Then a typical transmission begins with a start and ends with a stop, (with some possible restarts in between). Inside a transaction, there are only bytes separated by acknowledge.

Data on SDA are not authorized to change when SCL is high, except for the start and stop bits.

10.5.1 TWI Protocol

A write or read access is initiated by the master by sending a start bit. During the 7 next SCL cycles, the master sends on the SDA line the 7-bit slave address (example: Sensor: h12), MSB first. The next bit determines if the master request is a read or a write: when this bit is set to "0", a write action is requested. When it is set to "1", a read action is requested.

The slave device checks its address and sends an acknowledge bit back to the master. Write sequence (see Figures 10-1 and Figure 10-2 on page 60).

10.5.1.1 Write Sequence

As described below, the master sends the start bit, followed by the 7-bit slave address, followed by "0". Then the slave acknowledges.

The next byte sent by master must contain the address of the register to write to (MSB first). After the eighth bit has been received, the slave sends an acknowledge bit. Next, the master sends the data to write to the addressed register (MSB first). The sensor contains 8-bit or 16-bit registers. A 16-bit write is performed by sending two bytes (most significant byte first). After each byte, the slave sends an acknowledge bit.

A burst mode is also available by sending N data bytes after the register address byte. The first byte will be stored at the specified register address, and the address is automatically incremented into the slave state machine. After each received byte, the slave sends an acknowledge bit.

The end of a write sequence is performed by the master sending a stop bit. Read Sequence (see Figures 10-3 and Figure 10-4 on page 61).

10.5.1.2 Read Sequence

A read sequence begins like a write sequence, until the master has sent the register address to read from (MSB first).

After the eighth bit has been received and acknowledged by the slave, the master sends a new start bit, called re-start bit (because it is not preceded by a stop bit). The master then sends the 7 bits slave addressed, followed by a "1". After the slave has acknowledged, it sends on the SDA line the addressed register data (MSB first). The master sends an acknowledge bit after each 8-bit data transfer (in case of 16-bit register read or burst mode). When not acknowledging, the master must tie the SDA data line high.

When all the needed data bytes have been red, the master closes the sequence by sending a no-acknowledge bit, followed by the stop bit.

10.5.2 General Reset Sequence

This is a special mode used by the slave to reset its internal registers bank.

1. First, the master sends a start bit, followed by the 8-bit code 00h.
2. The slave issues an acknowledge bit.
3. Next the master sends the code 06h.
4. The slave issues an acknowledge bit.
5. The master sends a stop bit in order to terminate the transfer.

10.5.3 Start Bit

The start bit is a high to low transition on SDA, while SCL is high. When the master issues a start bit, it takes control of the bus

10.5.4 Repeated start

A repeated start is a start signal generated by a master which has already taken the control of the TWI bus. It is used by the master to initiate a transfer with a new slave, or with the same slave, in the other communication mode (transmit or receive mode), without releasing the bus.

10.5.5 Stop Bit

The stop bit is a low to *high* transition on SDA, while SCL is high. The master which has generated it sets the bus free.

10.5.6 Acknowledge Bit

The transmitter of the acknowledge bit must tie the SDA line to low to perform an acknowledgement. The receiver of the acknowledge bit must release the SDA line to high because at this time, it is not the master of the TWI bus. The receiver then checks the acknowledgement by reading a “0” on SDA even when it ties SDA to high.

10.5.7 Not Acknowledge Bit

If the receiver of the acknowledgement reads a “1” on SDA line during acknowledge clock pulse, that means transmitter did not acknowledge. The no-acknowledge bit is used by the master to terminate a read action.

Figure 10-1. 8-bit Register Write Sequence

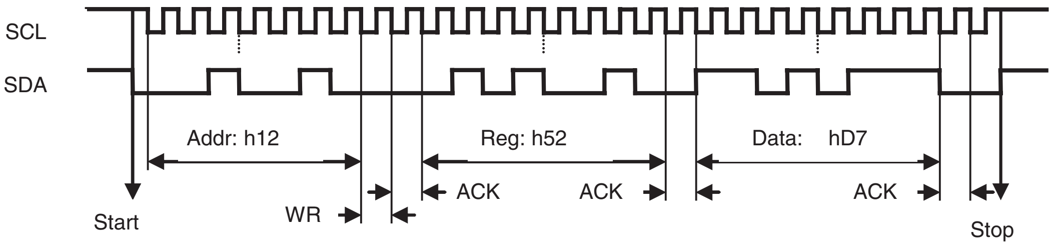


Figure 10-1 shows a single write sequence in the register h52 of the sensor. The 7bit sensor address is h12. The data put in this register is hD7. At each acknowledge, the slave drives SDA low and the master releases it.

Figure 10-2. 16-bit Register or 2-bytes-burst Write Sequence

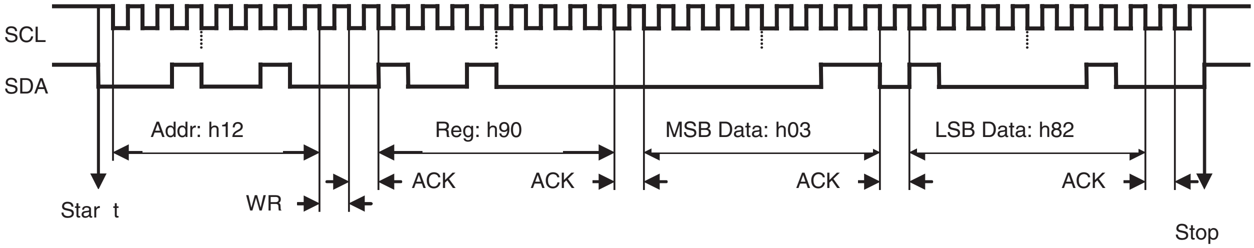


Figure 10-2 shows a 16-bit write sequence in the register h90 of the sensor. The 7bit sensor address is h12. The data put in this register is h0382. At each acknowledge, the slave drives SDA low and the master releases it. This mode could be used to write into two consecutive 8-bit registers (burst mode).

Figure 10-3. 8-bit Register Read Sequence

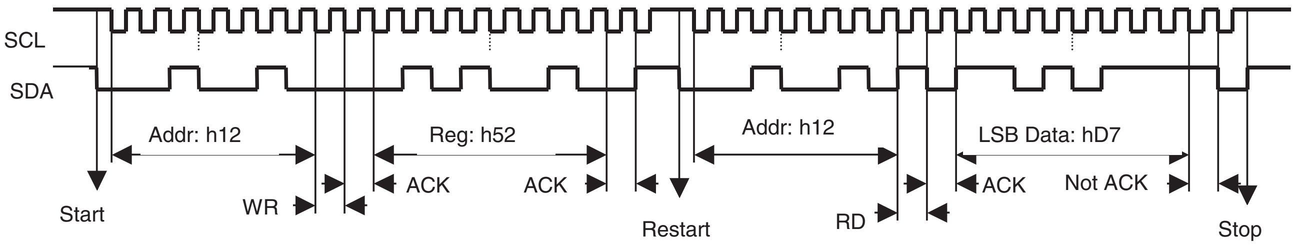


Figure 10-3 shows a single read sequence from the register h52 of the sensor. The 7-bit sensor address is h12. The data read from this register is hD7. At each acknowledge, the master drives SDA low (except for the last one) and the slave releases it.

Figure 10-4. 16-bit Register or 2-bytes-burst Read Sequence

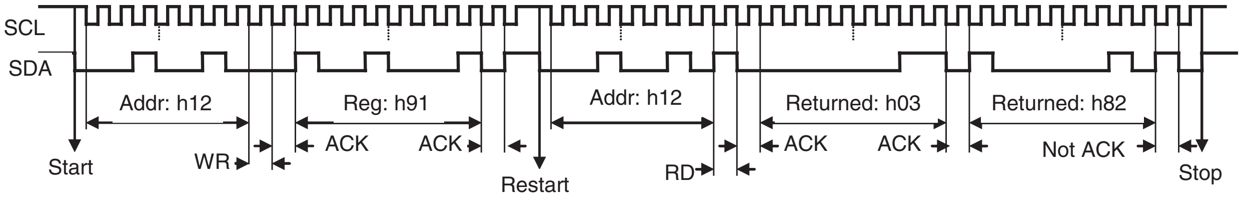


Figure 10-4 shows a 16-bit read sequence from the register h91 of the sensor. The 7bit sensor address is h12. The data read from this register is h0382. At each acknowledge, the master drives SDA low (except for the last one) and the master releases it. This mode could be used to read from two consecutive 8-bit registers (burst mode).

10.5.8 TWI Timings

Table 10-5. TWI Timings

Parameter	Symbol	Min	Max	Units
SCL clock frequency	^{t}SCL	0	400	kHz
Hold time for start and repeated start	^{t}STAH	600		ns
Set-up time for repeated start	^{t}STAS	600		ns
Set-up time for stop condition	^{t}STOS	600		ns
Data Hold time	^{t}DATH	100		ns
Data set-up time	^{t}DATS	100		ns
SDA and SCL rise time	^{t}r	20	300	ns
SDA and SCL fall time	^{t}f	20	300	ns
Bus free time between stop and start	^{t}FR	1300		ns

Figure 10-5. Start/Restart/Stop Conditions Timings

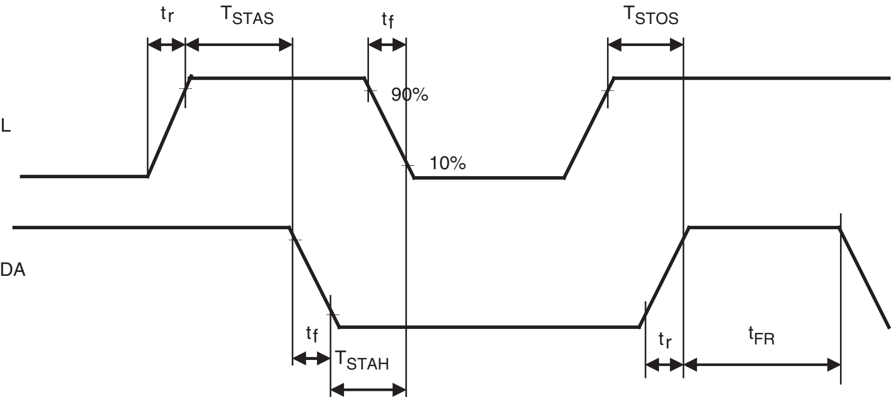
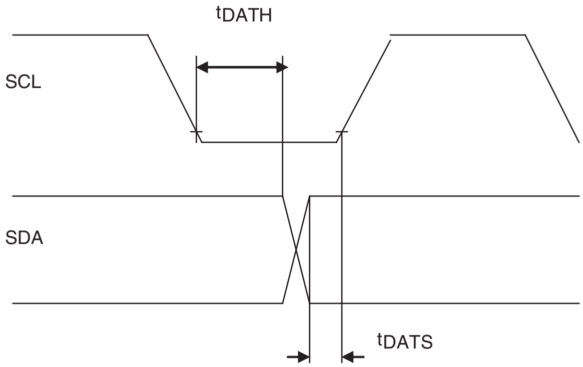


Figure 10-6. Data Relative To Clock Timings



10.6 Feedback

Several TWI registers might be used to control the sensor status, (see Section 10.4.1.11 and Section 10.4.2.10).

11. Power Management

11.1 Internal Clock Divider

The sensor must be fed by a master clock at 48 MHz.

The internal clock might be divided by 1, 2 or 4 internally to allow output frequency reduction. Use div_clk[1:0] (see Section 10.4.1.3).

Note that the internal clock divider doesn't have any effect on integration time (except on minimum integration time), waiting time or FL_delay.

11.2 Standby Mode

Standby mode might be controlled either via a pin or via a TWI register. Setting one of these two controls to active will put the sensor in standby mode at the end of current frame readout.

At power-up or after a reset the sensor is in standby mode.

11.2.1 Standby by TWI Register

See Section 10.4.1.8

11.2.2 Standby by Input Pin

To be active the standby pin must be enabled. It can be active at high or at low level, pad_stdby_ena & pad_stdby_inv (see Section 10.4.1.7).

The minimum duration of standby signal is 20 Master clock periods.

11.3 Idle Mode

In Idle mode, the sensor is waiting for a trigger signal

12. 3X3 Filter

Each filtered pixel output of the array is the result of a single multiplication of its surrounding 3x3 pixel square (9 pixels) with 9 coefficients. Border ROI pixels won't be filtered because they miss neighbors.

The 3x3 block might be bypassed using bypass_f33 (see Section 10.4.1.8).

12.1 Definition

Table 12-1. 3x3 coefficient matrix

C(–1,–1)	C(0,–1)	C(1,–1)
C(–1,0)	C(0,0)	C(1,0)
C(–1,1)	C(0,1)	C(1,1)

Table 12-2. Pixel Value Matrix, Centered on P(i,j) (i column and j line)

P(i-1,j-1)	P(i,j-1)	P(i+1,j-1)
P(i-1,j)	P(i,j)	P(i+1,j)
P(i-1,j+1)	P(i,j+1)	P(i+1,j+1)

Table 12-3. First Step: Product For Each Point of Coefficient By Pixel Value

C(–1,–1) x P(i-1,j-1)	C(0,–1) x P(i,j-1)	C(1,–1) x P(i+1,j-1)
C(–1,0) x P(i-1,j)	C(0,0) x P(i,j)	C(1,0) x P(i+1,j)
C(–1,1) x P(i-1,j+1)	C(0,1)x P(i,j+1)	C(1,1) x P(i+1,j+1)

Filter result on P(i,j):

$$Out_{(i,\ j)} = \frac{1}{2^B} \times \sum_{k=-1}^{1} \sum_{g=-1}^{1} (C_{(k,\ g)} \times P_{(i+k,\ j+g)})$$

Parameter explanation:

- Nine coefficients: $C_{(k,g)}$ <range –128 to +127> *see f33_coef_ij* (see Section 10.4.1.2).
- One shift value B: <range 0 to 12> *see f33_b_shift[3:0]* (see Section 10.4.1.1).
- One output value: Out <range 0 to 255> without sign or Out <range –128 to +127> with sign. see *f33_signed_filtout* (see Section 10.4.1.1).

$\text{Out}_{(i,j)}$ is computed on:

8 [image bit depth]

+ (7+1) [coefficient bit depth + sign]

+ 4 [bit due to the 9 factors]

= 19bit + sign

2's complement binary format:

Signed (2's complement)		Unsigned	
Decimal	**Binary**	**Decimal**	**Binary**
+127	0111 1111	+127	0111 1111
0	0000 0000	0	0000 0000
–1	1111 1111	+255	1111 1111
–128	1000 0000	+128	1000 0000

12.2 Saturation

Signed mode

- If out < -2^7 then filter out = -2^7
- If out > (2^7-1) then filter out = (2^7-1)

Unsigned mode

- If out < 0 then filter out = 0
- If out > (2^8-1) then filter out = (2^8-1)

12.3 Detailed Examples

Table 12-4. Detailed Examples

Output on 19+1 bit Naming sign S and each bit a, b, c…					FILTER OUT							
					B = 0				B = 2			
					Signed		Unsigned		Signed		Unsigned	
Sabc	defi	jklm	nopq	rstu	Sopq	rstu	nopq	rstu	Smno	pqrs	lmno	pqrs
0000	0000	0000	0010	1101	0010	1101	0010	1101	0000	1011	0000	1011
0000	0000	0000	1010	1101	🟥 0111	🟥 1111	1010	1101	0010	1011	0010	1011
0000	0000	0001	1010	1101	🟥 0111	🟥 1111	🟥 1111	🟥 1111	0110	1011	0110	1011
0000	0000	0010	0010	1101	🟥 0111	🟥 1111	🟥 1111	🟥 1111	🟥 0111	🟥 1111	1000	1011
0000	0001	0010	0010	1101	🟥 0111	🟥 1111	🟥 1111	🟥 1111	🟥 0111	🟥 1111	🟥 1111	🟥 1111
1111	1111	1111	1100	1010	1100	1010	🟨 0000	🟨 0000	1111	0010	🟨 0000	🟨 0000
1111	1111	1110	0100	1010	🟦 1000	🟦 0000	🟨 0000	🟨 0000	1001	0010	🟨 0000	🟨 0000
1111	1111	1101	1100	1010	🟦 1000	🟦 0000	🟨 0000	🟨 0000	🟦 1000	🟦 0000	🟨 0000	🟨 0000

Saturation: 🟥 Max value 🟦 Min value 🟨 Truncated to zero

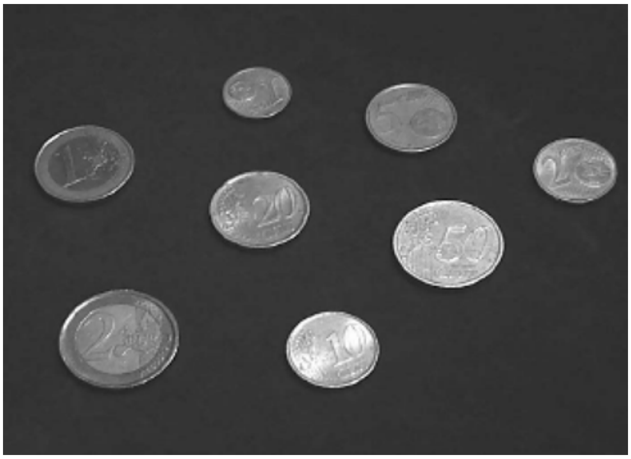
12.4 Output

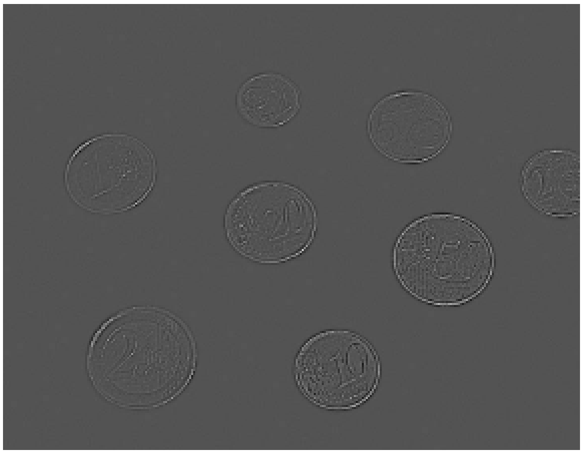
The filtered output is synchronized with the standard output. Pixel P(ij) is output on the same pixel clock as the filtered $P_{(i,j)}$.

Note that on the filtered output, one line at the top, one line at the bottom, one column on the left and one column on the right are left black.

12.4.1 3x3 Embeded Filter Use Example

The two outputs are read simultaneously





13. Gamma Correction

13.1 Principle

The gamma $(\gamma\ )$ correction algorithm might be used to correct the screen gamma as the sensor has a linear response. The screen is supposed to have a response: $Y\ =\ \alpha\times\ X^{\gamma}$

The correction is made with the law: $Y\text{corrected}\ =\ Y^{\frac{1}{\gamma}}$

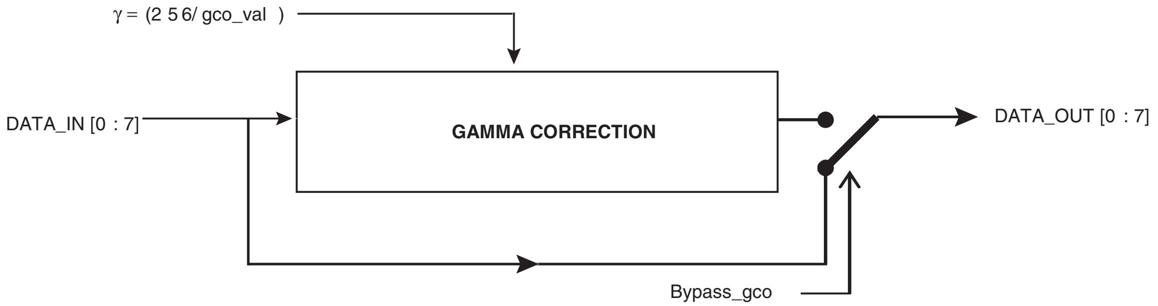
If gamma correction is not needed it is best to bypass it.

13.2 Control

Two TWI register might be used to control the **gamma correction**:

- *gco_val* (see Section 10.4.2.8)
- *bypass_gco* (see Section 10.4.1.8)

Figure 13-1. Gamma Correction



The correction is performed in the digital domain:

$$\text{DATA\_OUT}=\ 256\times\left(\frac{\text{DATA\_IN}}{256}\right)^{\frac{256}{\text{gco\_val}}}$$

14. Mux Out

14.1 Mask

Two registers might be used to mask:

- Either the LEN during inactive part of FEN signal *mask_idle_len* (see Section 10.4.1.3)
- Or data when FEN or LEN are inactive see *mask_idle_data* (see Section 10.4.1.3)

14.2 Input/Output

14.2.1 Dig In/Dig Out - Input/Output Specification

Table 14-1. I/O Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VIL	Input low voltage	-0.3		0.35 x VDD18D	Volts	
VIH	Input high voltage	0.65 x VDD18D		VDD18D + 0.3V	Volts	
VOL	Output low voltage			0.45	Volts	VDD18D = min, IOL = –2 mA
VOH	Output high voltage	VDD18D-0.45			Volts	VDD18D = min, IOH = 2 mA
VTH	Input hysteresis voltage		0.25		Volts	
IILPU	Input low current for PU pins			200	µA	VIL = VSS
IIHPU	Input high current for PU pins	–1	0	1	µA	VIH = VDD18D
IILPD	input low current for PD pins	–1	0	1	µA	VIL = VSS
IIHPD	Input high current For PD pins	–200			µA	VIH = VDD18D
IIL	Input low current	–1	0	1	µA	VIL = VSS
IIH	Input high current	–1	0	1	µA	VIH = VDD18D
CIN	Input pin capacitance		5	10	pF	

Note: PD stands for pull down, PU for pull up.

14.2.2 TWI Input Output Specification

Table 14-2. TWI Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VIL_{TWI}	Input low voltage	-0.3		0.3 x VDD18D	Volts	
VIH_{TWI}	Input high voltage	0.7 x VDD18D			Volts	
VOL3	Output low voltage			0.2 x VDD18D	Volts	at 3mA sink current
CIN_{TWI}	Input pin capacitance		5	10	pF	

14.2.3 Output in High Impedance

All the outputs can be set to high impedance. There is no possibility to set some outputs at HiZ level and others in active mode, (see Section 10.4.1.8).

15. Sensor I/O

15.1 I/O LIST

Table 15-1. Pinout

Label	Description	Type	Pin Number
D3	Data	Dig OUT	1
D2	Data	Dig OUT	2
CLKREF	48 MHz	Dig IN	3
GND18D	Digital ground	Ground	4-7-22-45
VDD18D	Digital power	Power	5-8-23-46
D1	Data	Dig OUT	6
GND18D	Digital ground	Ground	4-7-22-45
VDD18D	Digital power	Power	5-8-23-46
D0	Data LSB	Dig OUT	9
DATA-CLK	Data clock	Dig OUT	10
F0	Filter out LSB	Dig OUT	11
F1	Filter out	Dig OUT	12
F2	Filter out	Dig OUT	13
F3	Filter out	Dig OUT	14
F4	Filter out	Dig OUT	15
F5	Filter out	Dig OUT	16
F6	Filter out	Dig OUT	17
F7	Filter out MSB	Dig OUT	18
LEN	Line enable	Dig OUT	19
FEN	Frame enable	Dig OUT	20
FLO	External illumination control	Dig OUT	21
GND18D	Digital ground	Ground	4-7-22-45
VDD18D	Digital power	Power	5-8-23-46
TRIG	Snap Shot control input	Dig IN PU	24
Standby	Standby control	Dig IN PU	25
RESETB	Reset control	Dig IN	26
SCAN-MODE	For test purpose	Ground	27
A0 TWI	TWI address LSB	Dig IN	28
A1 TWI	TWI address	Dig IN	29
VLR	For test purpose	DNC	30
VsigP	For test purpose	Ground	31
ATESTV	For test purpose	DNC	32

Table 15-1. Pinout (Continued)

Label	Description	Type	Pin Number
ATESTI	For test purpose	DNC	33
ADC_REF	Connected to external resistor	Ana IN	36
		NC	37
GND33A	Analog ground	Ground	34-38
VDD33A	Analog power	Power	35-39
VDD18A	Analog power	Power	40
SDA	TWI data	TWI	41
SCL	TWI clock	TWI	42
D7	Data MSB	Dig OUT	43
D6	Data	Dig OUT	44
GND18D	Digital ground	Ground	4-7-22-45
VDD18D	Digital power	Power	5-8-23-46
D5	Data	Dig OUT	47
D4	Data	Dig OUT	48

Notes: 1. All power with the same name must be connected to the same power supply.

2. All grounds must be connected.

3. DNC stands for do not connect, NC for not connected.

15.2 Power Supply

Table 15-2. Power Supply

		Value			
Parameter	Symbol	Min	Typ	Max	Unit
Analog Power supply relative to GND level	VDD33A	3.0	3.3	3.6	V
Digital Power supply relative to GND level	VDD18D	1.6	1.8	2.0	V
Digital Power supply relative to GND level	VDD18A	1.6	1.8	2.0	V
Supply current at 60 fps (VDD33A pin)	AIDD		13		mA
Supply current at 60 fps (VDD18D pins)	DIDD		18		mA
Supply current at 60 fps (VDD18A pin)	IDD18A		3		mA
Standby supply current (in VDD pin)(1)	IDDz		50		µA
Power dissipation	P		80		mW

Note: 1. $\sum(AI_{DD} + DI_{DD})$ with TWI on, without communication and without CLKREF input.

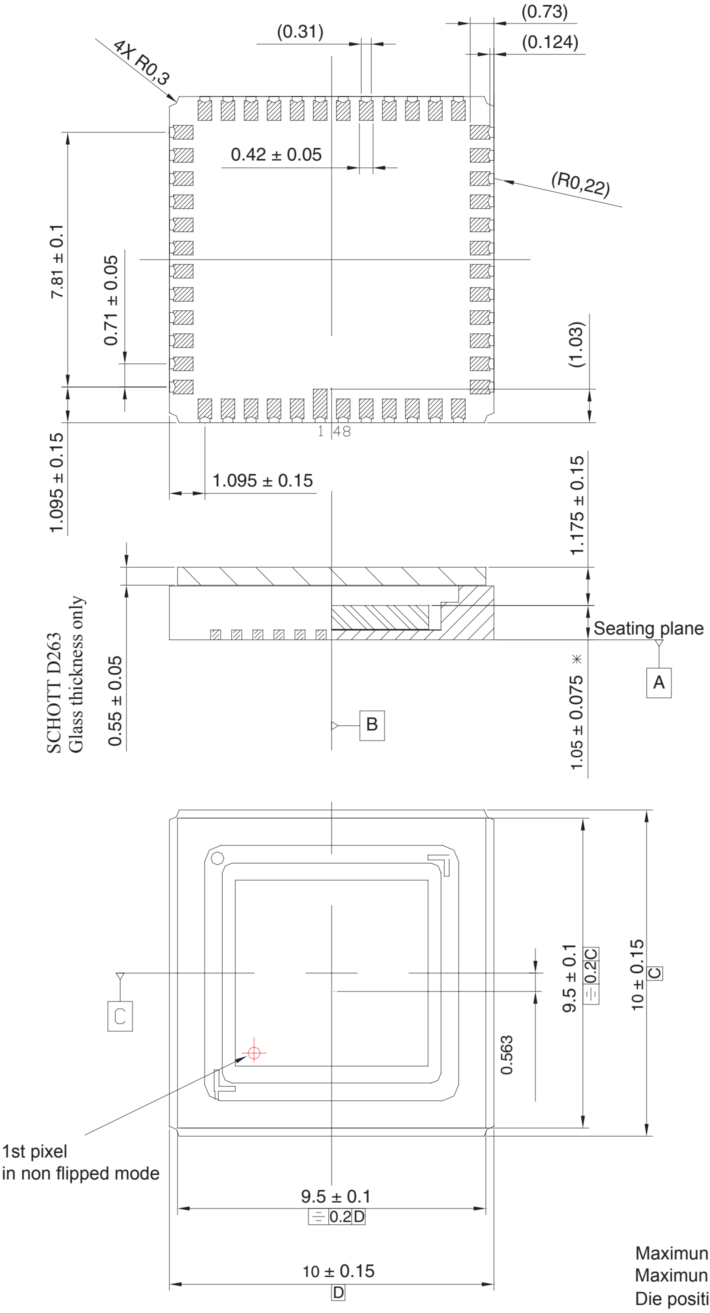
15.3 Input Clock

Table 15-3. Clock Input/Output

Parameter	Value			
	Min	**Typ**	**Max**	**Unit**
CLKREF input	48 - 0.5%	48	48 + 0.5%	MHz
Duty cycle on CLKREF	40	50	60	%
DATA-CLK with clock divider = 1	CLKREF			MHz
DATA-CLK with clock divider = 2	CLKREF/2			MHz
DATA-CLK with clock divider = 4	CLKREF/4			MHz

16. Drawings

Figure 16-1. Mechanical Drawing (in mm)



note: Plating
Ni : 1.27~8.89 µ
Au: 0.50 µ min

Maximun tilt of image area diagonal to seating plane ref A: 50 µm
Maximun rotation of image area to ref B and C: 1°
Die positioning to ref B and C : +/-125 µm

* Not including the tilt specification

Figure 16-2. Pinout Position (Top View)

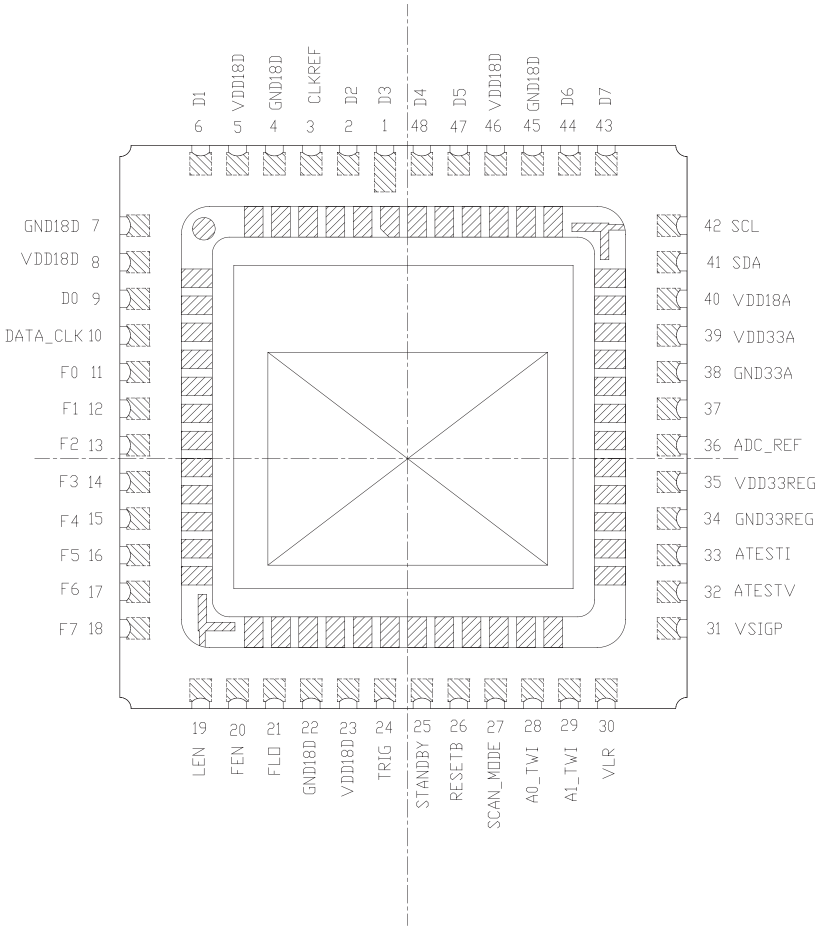


Figure 16-3. Footprint

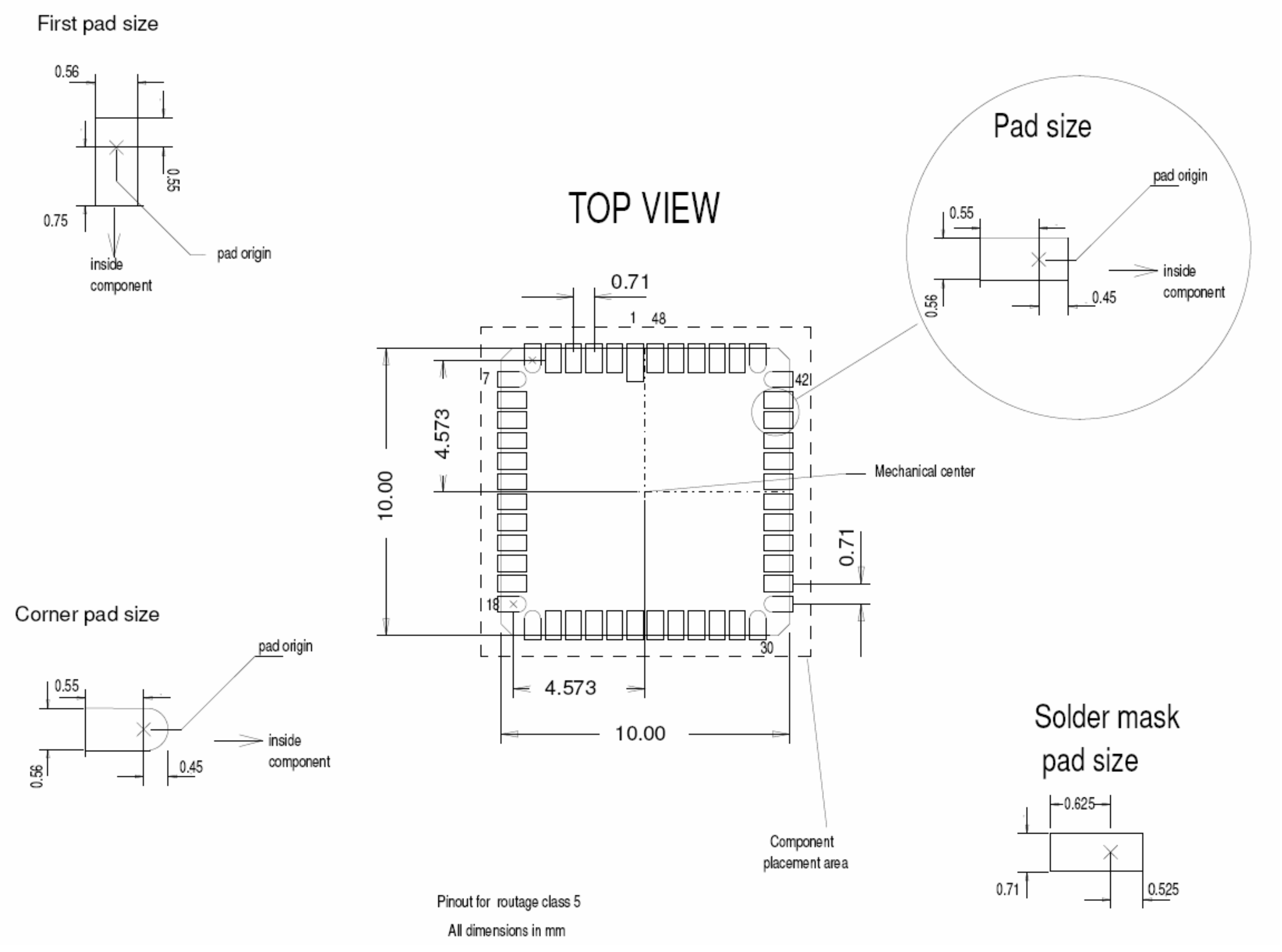


Figure 16-4. Jedec Tray Drawing (160 parts per tray)

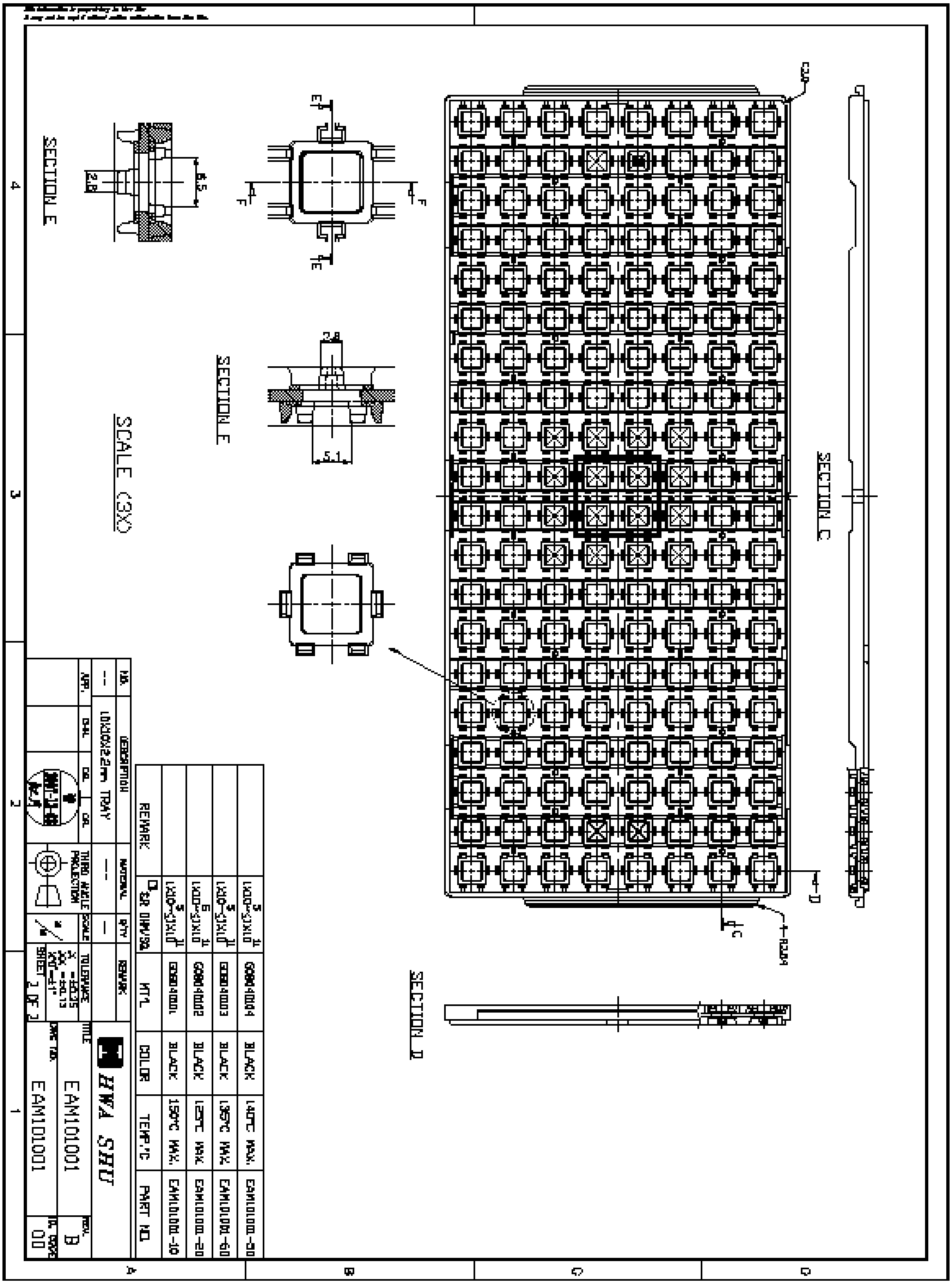
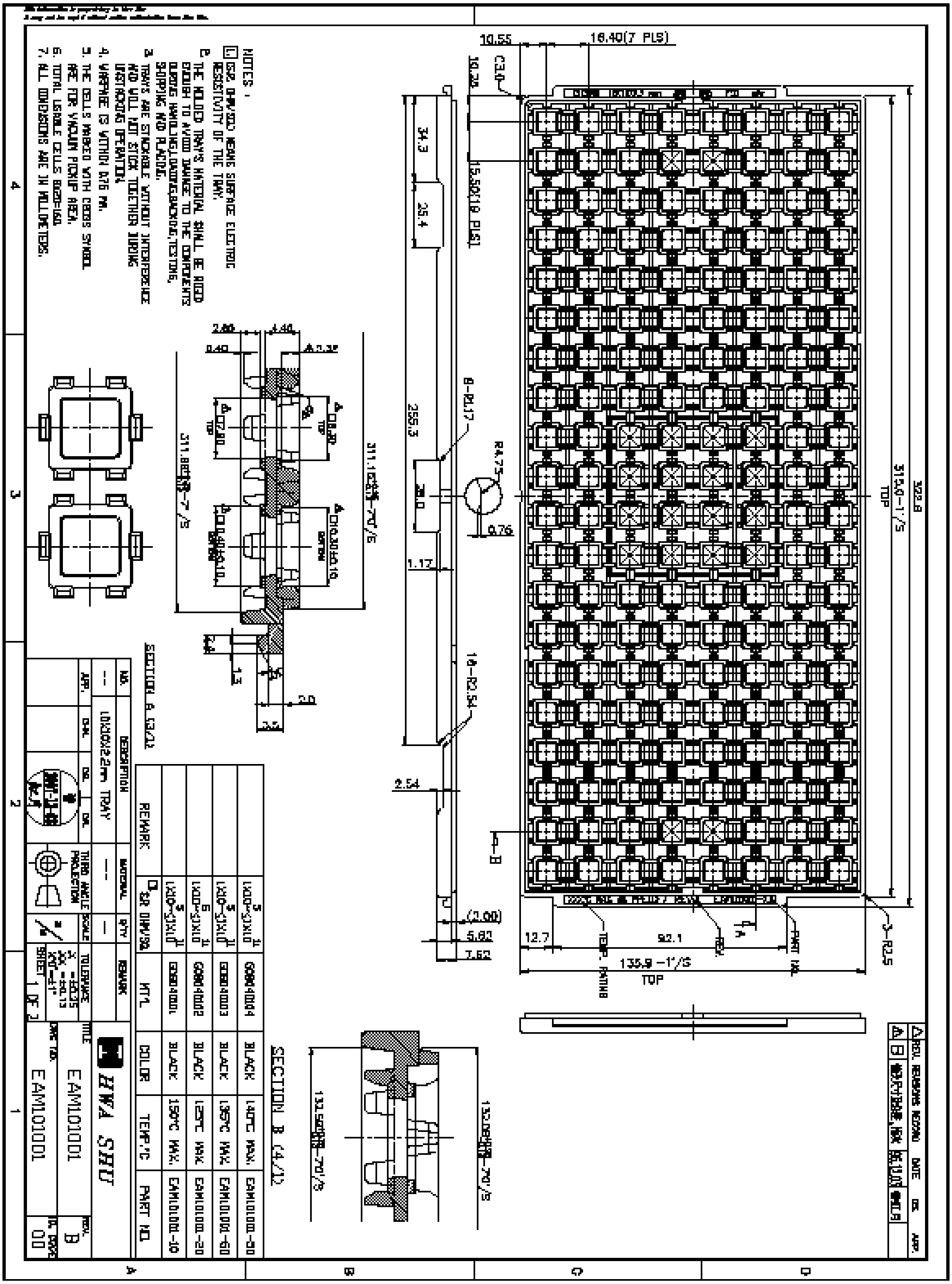


Figure 16-5. Jedec Tray Drawing (part 2)


NOTES :
ESD DAMAGED MEANS SURFACE ELECTRIC RESISTIVITY OF THE TRAY.
THE MOLDED TRAY'S MATERIAL SHALL BE RIGID ENOUGH TO AVOID DAMAGE TO THE COMPONENTS DURING HANDLING, LOADING, BACKING, TESTING, SHIPPING AND PLACING.
TRAYS ARE STACKABLE WITHOUT INTERFERENCE AND WILL NOT STICK TOGETHER DURING UNSTACKING OPERATION.
4. WARPAGE IS WITHIN 0.76 MM.
5. THE CELLS MARKED WITH CROSS SYMBOL ARE FOR VACUUM PICKUP AREA.
6. TOTAL USABLE CELLS 8x20=160.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
SECTION A (3/1)
SECTION B (4/1)
10.55
16.40(7 PLS)
15.50(19 PLS)
34.3
25.4
255.3
28.0
1.17
2.54
12.7
92.1
135.9
TOP
315.0
322.6
R4.75
0.76
2.00
5.62
7.62
2.0
1.3
HWA SHU
EAM101001
10x10x2.2mm TRAY
REMARK
MT'L
COLOR
TEMP ℃
PART NO.
BLACK
150℃ MAX.
EAM101001-10
EAM101001-20
EAM101001-60
EAM101001-30
THIRD ANGLE PROJECTION
SHEET 1 OF 2
B
A
B
C
D
1
2
3
4

Note: e2v will use EAM101001-10 (150°C) to deliver the EV76C454 product.

17. Ordering Codes

- EV76C454BBT-EQV for black and white option
- EV76C454BMT-EQV for WRGB CFA option
- EV76C454BCT-EQV for Bayer CFA option

For more information on other packaging or other CFA please contact e2v.

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