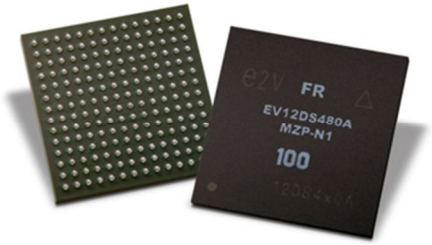
EV12DS480AZP
Low power 12-bit 8GSps Digital to Analog Converter with 4/2:1 Multiplexer
Datasheet DS 60S 217580 rev A.1



MAIN FEATURES

- 12-bit resolution
- 6.4 GSps guaranteed conversion rate (operational up to 7 GSps)
- 8.0 GSps guaranteed conversion with reduced data rate (operational up to 8.5 GSps)
- –3 dB Analog output Bandwidth of 7.5 GHz (30 ps rise and fall time on DAC output step response)
- Support RF signal synthesis up to 12 GHz (X-band)
- Support RF signal synthesis up to 24 GHz (with reduced output power)
- 4:1 or 2:1 integrated parallel MUX (selectable)
- Selectable output modes:
  Return To Zero (RTZ), Non Return to Zero (NRZ), Narrow Return To Zero (NRTZ) and Radio Frequency (RF)
- Low latency time: 3 clock cycles
- 2.6 Watt Power Dissipation (in 4:1 MUX)
- 3 Wires Serial Interface
- LVDS differential data input and DSP clock output.
- Functions:
  - Selectable MUX ratio 4:1 (up to 8.0 GSps), 2:1 (up to 3.2 GSps)
  - User-friendly functions, digitally controlled through a 3WSI serial interface:
    - Gain Adjustment
    - Output clock division selection (possibility to change the division ratio of the DSP clock) (OCDS)
    - Reshaped Pulse Width (RPW) and Reshaped Pulse Begin (RPB) adjustments for performance optimization
    - Clock phase shift select for synchronization with DSP (PSS[2:0])
    - Input Under Clocking Mode by 1/2/4 (IUCM)
    - Direct access available for bit OCDS and PSS
    - Input data check bit for timing interface with FPGA check (IDC)
    - Timing violation flag (setup or hold) for FPGA
    - communication monitoring (TVF)
- Analog output differential swing: 1Vpp (100Ω differential impedance)
- External SYNC that can be used for synchronization of multiple DACs
- Power supplies: 3.3 V (Digital), 3.3V & 5V (Analog)
- FpBGA package (15 x 15 mm body size, 1 mm pitch)
- DOCSIS 3.0 Compatible

PERFORMANCE @ 6.4 GSps

- SFDR
  - 1st Nyquist (NRTZ - 3136 MHz): SFDR = 60 dBc
  - 2nd Nyquist (NRTZ - 6336 MHz): SFDR = 53 dBc
  - 3rd Nyquist (RF - 9536 MHz): SFDR = 50 dBc
  - 4th Nyquist (RF - 12736 MHz): SFDR = 50 dBc
  - 7th Nyquist (RF - 19136 MHz): SFDR = 43 dBc
  - 8th Nyquist (RF - 25536 MHz): SFDR = 44 dBc
- IMD3 Dual-tone
  - 1st Nyquist (NRTZ - 2950 & 2960 MHz): 70 dBc
  - 2nd Nyquist (RF - 6150 & 6160 MHz): 67 dBc
  - 3rd Nyquist (RF - 9150 & 9160 MHz): 55 dBc
  - 4th Nyquist (RF - 12550 & 12560 MHz): 56 dBc
- Broadband NPR at -14 dBFS Loading Factor (90% of full Nyquist zone) = 2880MHz
  - 1st Nyquist (NRTZ): NPR = 43,3 dB, 8.7 Bit Equivalent
  - 2nd Nyquist (NRTZ): NPR = 38 dB, 7,85 Bit Equivalent
  - 3rd Nyquist (RF): NPR = 35,4 dB, 7.4 Bit Equivalent

PERFORMANCE @ 8.0 GSps with reduced data rate

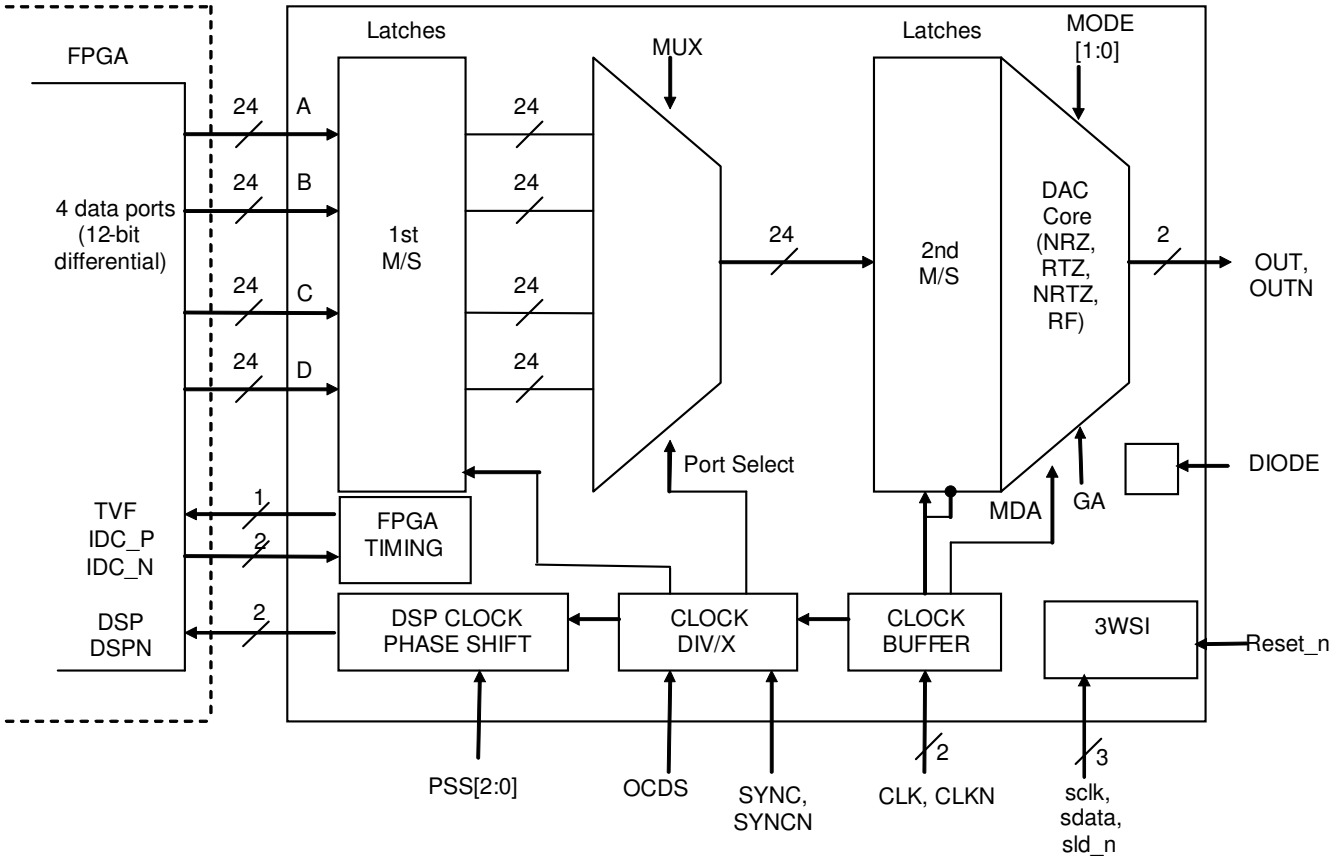
- Broadband NPR at -14 dBFS Loading Factor (90% of full Nyquist zone), RF mode :
  - With IUCM2: 5st Nyquist (8-10 GHz): NPR = 35dB, 7,35 Bit Equivalent
  - With IUCM4 : 9th Nyquist (8-9 GHz): NPR = 38 dB, 7,85 Bit Equivalent
- SFDR
  - With IUCM2 : 5st Nyquist (RF - 8040 MHz): SFDR = 54 dBc
  - With IUCM4 : 9th Nyquist (RF - 8020 MHz): SFDR = 58 dBc

Available in NASA Level 1, ECSS Class 3, Military, Industrial and Commercial Grade.

Teledyne e2v Semiconductors SAS, avenue de Rochepleine 38120 Saint-Egrève, France Holding Company: Teledyne e2v Semiconductors SAS
Telephone: +33 (0)4 76 58 30 00
Contact Teledyne e2v by e-mail: hotline-bdc@teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

1 BLOCK DIAGRAM

Figure 1. Simplified block diagram



2 DESCRIPTION

The EV12DS480A is a 12-bit 8.0 GSps DAC with an integrated 4:1 or 2:1 multiplexer and 7.5 GHz output bandwidth, allowing easy interface with standard FPGAs thanks to user friendly features such as DSP clock, OCDS, PSS, TVF, IUCM.

It embeds 4 different output modes (NRZ, RTZ, NRTZ and RF) that allow performance optimizations depending on the Nyquist zone of interest.

3 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum ratings

Table 1. Absolute maximum ratings

Parameter	Symbol	Value		Unit
		min	max	
VCCA5 analog supply voltage	VCCA5	–0.6	6.0	V
VCCA3 analog supply voltage	VCCA3	–0.6	4.0	V
VCCD digital supply voltage	VCCD	–0.6	4.0	V
Digital input (on each single-ended input), IDC and SYNC signal	[P0..P11], [P0N..P11N], IDC_P, IDC_N, SYNC, SYNCN	0	VCCA3	V
Digital input maximum differential swing Port P = A, B, C, D			2.0	Vpp
Master clock input (on each single ended input)	CLK, CLKN	1.0	4.0	V
Master clock maximum differential swing			3	Vpp
Control function inputs voltage	PSS[0..2], OCDS, reset_n, sclk, sdata, sld_n	–0.4	VCCD + 0.4	V
Junction temperature	T_J		170	°C

Parameter	Symbol	Value	Unit
Electrostatic discharge human body model	ESD HBM	JESD22-A114-E Class 1C (1000V to < 2000V)	V
Electrostatic discharge machine model	ESD MM	JESD22-A115-C Class M2 (100V to < 200V)	
Latch up		JEDEC 78B Class I & Class II	
Moisture sensitivity level	MSL	3	
Storage temperature range	Tstg	–65 to +150	°C

Notes:

1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
2. All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
3. Maximum ratings enable active inputs with DAC powered off.
4. Maximum ratings enable floating inputs with DAC powered on.
5. DSP clock and TVF output buffers must not be shorted to ground or positive power supply.

3.2 Recommended conditions of use

Table 2. Recommended conditions of use

Parameter	Symbol	Recommended Value	Unit	Note
V_{CCA5} analog supply voltage	V_{CCA5}	5.0	V	(1) (2)
V_{CCA3} analog supply voltage	V_{CCA3}	3.3	V	(1) (2)
V_{CCD} digital supply voltage	V_{CCD}	3.3	V	(1) (2)
Digital input (on each single ended input), IDC and SYNC signal Port P = A, B, C, D V_{IL} V_{IH} Digital input differential swing	$[P_0..P_{11}]$, $[P_{0N}..P1_{1N}]$, IDC_P, IDC_N, SYNC, SYNCN	 1.075 1.425 350	 V V mVp	
Master Clock input differential mode swing	CLK, CLKN	1.4	Vpp	
Master Clock input power level (differential mode)	P_{CLK}	4	dBm	(3)
Control function inputs V_{IL} V_{IH}	PSS[0..2], OCDS, reset_n, sclk, sdata, sld_n	 0 V_{CCD}	 V V	
RPB & RPW settings for enhanced dynamic performance 6.4 GSps in NRTZ mode	RPB RPW	RPB2 RPW0	– –	(4)
RPB & RPW settings for enhanced dynamic performance 6.4 GSps in RF mode	RPB RPW	RPB1 RPW0	– –	(4)
RPB & RPW settings for enhanced dynamic performance 8.0 GSps (IUCM4) in RF mode	RPB RPW	RPB1 RPW2	– –	(4)

Notes:

1. See Section 7.8 for power on requirement
2. No power-down sequencing is required
3. Clock input power can be decreased when clock frequency is lower as long as it respects the specification.
4. A good compromise for RPB & RPW values is defined for a 6.4 GHz and 8.0 GHz clock frequency. This couple of values depends on the clock frequency. These recommended RPB/RPW couples have been chosen to offer good performance over the Nyquist of use (1st and 2nd in NRTZ mode, 2nd and 3rd in RF mode at Fclock = 6.4 GHz and for 8th and 9th Nyquist at Fclock = 8.0 GHz). For specific condition (for example looking at the SFDR at a particular output frequency), a RPB/RPW optimization can significantly increase performance.

3.3 DC Electrical Characteristics

Unless otherwise specified:

Values in the table below are given over temperature range with typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), with 4:1 MUX ratio, typical swing on input data, typical Pclk, master clock input jitter is below 100 fs rms integrated over 11 GHz bandwidth.

Min and Max values are given over temperature range. Typ values are given at ambient temperature.

Table 3. DC Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
RESOLUTION			**12**		**bit**		
POWER REQUIREMENTS							
Power Supply voltage							
- Analog	V_{CCA5}	4.75	5	5.25	V		
- Analog	V_{CCA3}	3.15	3.3	3.45	V		1, 6
- Digital	V_{CCD}	3.15	3.3	3.45	V	(2)	
Power Supply current (4:1 MUX)							
- Analog	I_{CCA5}	85	100	120	mA		
- Analog	I_{CCA3}	170	205	240	mA		1, 6
- Digital	I_{CCD}	340	425	490	mA	(8)	
Power Supply current (2:1 MUX)							
- Analog	I_{CCA5}	85	100	120	mA		
- Analog	I_{CCA3}	165	205	240	mA		1, 6
- Digital	I_{CCD}	300	370	430	mA	(8)	
Power dissipation (4:1 MUX)	PD4	2.2	2.6	3	W	(8)	1, 6
Power dissipation (2:1 MUX)	PD2	2.0	2.4	2.8	W	(8)	1, 6
DIGITAL DATA INPUTS, SYNC and IDC INPUTS							
Logic compatibility			LVDS				
Digital input voltages:							
- Differential input voltage	VID	100	350	500	mVp		1, 6
- Common mode	VICM	1	1.25	1.6	V		1, 6
Input capacitance from each single input to ground				2	pF		5
Differential input resistance		80	100	120	Ω		1, 6
CLOCK INPUTS							
Input voltages (Differential operation swing)		0.6	1.4	2.4	Vpp		1, 6
Power level (Differential operation)		–4	4	+8.5	dBm	(3)	1, 6
Common mode		2.4	2.5	2.6	V		1, 6
Input capacitance from each single input to ground (at die level)				2	pF		5
Differential Input resistance:		80	100	120	Ω		1, 6
DSP CLOCK OUTPUT							
Logic compatibility			LVDS				
Output voltages:							
- Differential output voltage	VOD	100	350	450	mVp		1, 6
- Common mode	VOCM	1.055	1.250	1.375	V	(10)	1, 6
ANALOG OUTPUT							
Full-scale Differential output voltage (100Ω differentially terminated)		0.89	1	1.08	Vpp		1, 6
Full-scale output power (differential output on 100Ω)			+1		dBm	(4)	1, 6
Single-ended mid-scale output voltage (50Ω terminated)		V_{CCA5}–0.50	V_{CCA5}–0.43	V_{CCA5}–0.36	V	(5)	1, 6

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Output capacitance			1.5		pF		5
Nominal Output internal differential resistance		90	100	110	Ω		1, 6
Output VSWR (using Teledyne e2v's evaluation board) 2.25 GHz 4.5 GHz 6.0 GHz 8.0 GHz			 1.2 1.4 TBD TBD				 4
–3 dB Analog Output bandwidth			7.5		GHz		4
FUNCTIONS							
Digital functions: sdata, sld_n, sclk, reset_n, OCDS, PSS Logic 0 Logic 1	 VIL VIH	 1.6	 0 V_{CCD}	 0.8	 V V		 1, 6
sdata, sld_n, sclk, reset_n - Low Level input current - High Level input current	 IIL IIH	 –120 10	 –55 80	 –10 120	 µA µA		 1, 6
OCDS, PSS: - Low Level input current - High Level input current	 IIL IIH	 –150 50	 –100 100	 –50 150	 µA µA		 1, 6
Digital output function TVF Logic 0 Logic 1	VOL VOH IOL IOH	 1.5		 0.6 500 500	V V µA µA	 (8)	1, 6 5
DC ACCURACY							
Differential Non-Linearity	DNL+		0.4	0.95	LSB		1, 6
Differential Non-Linearity	DNL-	–0.95	–0.4		LSB		1, 6
Integral Non-Linearity	INL+		0.7	2.5	LSB		1, 6
Integral Non-Linearity	INL-	–2.5	–0.7		LSB		1, 6
DC GAIN							
DAC output voltage (@ default value)		0.89		1.08	Vpp	(6)	1, 6
DAC output voltage adjustment step		–5	0.3	+5	mV		1
DAC output voltage after optimum 3WSI adjustment		0.995	1	1.005	Vpp	(6)	1
DAC output voltage sensitivity to supplies			3.2	5	%	(7)	1
DAC output voltage drift over temperature			45	55	mVpp	(9)	4

Notes:

1. See Section 3.6 for explanation of test levels.
2. See Section 7.8 for power up sequencing.
3. For use in higher Nyquist zone, it is recommended to use higher power clock within the limit.
4. In NRZ mode only. For the other reshaped modes, the output power will be lower by construction. See Figure 9 and Figure 10.
5. These values are mainly for information as single-ended operation in not recommended.
6. The DAC output voltage can be adjusted close to 1Vpp thanks to the GAIN control register in the 3WSI.
7. DAC output voltage sensitivity to supplies = DAC output voltage at Vmax - DAC output at Vmin. Measurement done with DAC Gain Adjust at its default value (3WSI GA register default value = 0x200) Min and Max values are given versus supplies at room temperature
8. Tested with IOL & IOH = 500µA
9. DAC output voltage sensitivity to temperature = DAC output voltage at Tmax - DAC output voltage at Tmin. Measurement done with DAC Gain Adjust at its default value (3WSI GA register default value = 0x200) Min and Max values are given versus temperature with typical supplies
10. It has been noted that at extreme low temperature and/or V_{CCD} min, the swing of the DSP clock signal is reduced. However it stays above the 100mVp generally specified for LVDS input swing and thus should not be an issue at the system level.

3.4 AC Electrical Characteristics

Unless otherwise specified:

- Typical values in the table below are given at ambient temperature with typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), Min and Max values are given over temperature range.
- 4:1 MUX ratio, typical swing on input data, typical Pclk, master clock input jitter is below 100 fs rms integrated over 11 GHz bandwidth.

Important note on expected performance:

Figures for performance in NRTZ and RF modes are given for recommended value of RPW (Reshaping Pulse Width) and RPB (Reshape Pulse Begin). Tuning of RPW/RPB by customer is recommended. Generally, increasing RPW improves linearity (SFDR) at the expense of carrier output power (SNR). Decreasing RPW improves carrier output power (SNR) at the expense of linearity (SFDR).

Figures for performance in RTZ mode are given for the recommended value of RPB which are digitally programmable through the 3 Wires Serial Interface (3WSI).

Values between brackets are given for optimum RPB/RPW values. Optimum settings may differ from part to part.

For dual-tone results, RPB / RPW are tuned such as the intermodulation products (IMD3 to IMD9) values are minimized.

See Section 5.3 for more information on RPW and RPB settings. Recommended values for RPB and RPW are given in Table 3-2.

Table 4. AC Electrical Characteristics NRZ Mode (First Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX							
Fs = 6.4 GSps @ Fout = 64 MHz 0 dBFS			67				4
Fs = 6.4 GSps @ Fout = 3136 MHz 0 dBFS			51				4
Fs = 3.0 GSps @ Fout = 30 MHz 0 dBFS	|SFDR|	64	71		dBc	(2) (3)	1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0 dBFS		51	58				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0 dBFS			70				4
Fs = 3.2 GSps @ Fout = 1568 MHz 0 dBFS			55				4
Fs = 1.5 GSps @ Fout = 15 MHz 0 dBFS	|SFDR|	65	75		dBc	(2) (3)	1, 6
Fs = 1.5 GSps @ Fout = 735 MHz 0 dBFS		57	64				1, 6
Highest spur level							
4:1 MUX							
Fs = 6.4 GSps @ Fout = 64 MHz 0 dBFS			-70				4
Fs = 6.4 GSps @ Fout = 3136 MHz 0 dBFS			-59				4
Fs = 3.0 GSps @ Fout = 30 MHz 0 dBFS			–70		dBm		1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0 dBFS			–61				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0 dBFS			–70				4
Fs = 3.2 GSps @ Fout = 1568 MHz 0 dBFS			–60				4
Fs = 1.5 GSps @ Fout = 15 MHz 0 dBFS			–74		dBm		1, 6
Fs = 1.5 GSps @ Fout = 735 MHz 0 dBFS			–66				1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc/2 @ 6.4 GSps			-80		dBm		4
Fc/4 @ 6.4 GSps			-75		dBm		4
Self-Noise Density at code 0 or 4095 @ 6.4 GSps			<-160		dBm/Hz		4

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 6.4 GSps 3.136 GHz broadband pattern, 64 MHz notch width	NPR		41.4		dB	(4) (5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		8.4		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		52.4		dB		4
Noise Power Ratio –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	43	46		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.7	9.2		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	54	57		dB		1, 6

Notes:

1. See Section 3.6 or explanation of test levels.
2. Refer to Figure 84. SFDR vs temperature vs modes.
3. Refer to Figure 83. SFDR vs Power supplies vs modes.
4. Refer to Figure 109 for NPR variation versus temperature.
5. Refer to Figure 108 for NPR variation versus supplies.

Table 5. AC Electrical Characteristics NRTZ Mode (First & Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX							
Fs = 6.4 GSps @ Fout = 64 MHz 0 dBFS			(73)				4
Fs = 6.4 GSps @ Fout = 3136 MHz 0 dBFS			(60)				4
Fs = 6.4 GSps @ Fout = 6336 MHz 0 dBFS			(53)				4
Fs = 3.0 GSps @ Fout = 30 MHz 0 dBFS	|SFDR|	62	75		dBc		1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0 dBFS		60	65				1, 6
Fs = 3.0 GSps @ Fout = 2970 MHz 0 dBFS		55	60			(2) (3)	1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0 dBFS			76				4
Fs = 3.2 GSps @ Fout = 1568 MHz 0 dBFS			63				4
Fs = 3.2 GSps @ Fout = 3168 MHz 0 dBFS			62				4
Fs = 1.5 GSps @ Fout = 15 MHz 0 dBFS	|SFDR|	65	77		dBc		1, 6
Fs = 1.5 GSps @ Fout = 735 MHz 0 dBFS		60	73				1, 6
Fs = 1.5 GSps @ Fout = 1485 MHz 0 dBFS		51	57			(2) (3)	1, 6
Highest spur level (Single tone)							
4:1 MUX							
Fs = 6.4 GSps @ Fout = 64 MHz 0 dBFS			(-80)				4
Fs = 6.4 GSps @ Fout = 3136 MHz 0 dBFS			(-70)				4
Fs = 6.4 GSps @ Fout = 6336 MHz 0 dBFS			(-71)				4
Fs = 3.0 GSps @ Fout = 30 MHz 0 dBFS			–76		dBm		1, 6
Fs = 3.0 GSps @ Fout = 1470 MHz 0 dBFS			–69				1, 6
Fs = 3.0 GSps @ Fout = 2970 MHz 0 dBFS			–76				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 32 MHz 0 dBFS			–77				4
Fs = 3.2 GSps @ Fout = 1568 MHz 0 dBFS			–67				4
Fs = 3.2 GSps @ Fout = 3168 MHz 0 dBFS			–80				4
Fs = 1.5 GSps @ Fout = 15 MHz 0 dBFS			–76		dBm		1, 6
Fs = 1.5 GSps @ Fout = 735 MHz 0 dBFS			–76				1, 6
Fs = 1.5 GSps @ Fout = 1485 MHz 0 dBFS			–78				1, 6
Dual-tone over Full Nyquist							
4:1 MUX Fs = 6.4 GSps @ Fout1 = 2950 MHz, Fout2 = 2960 MHz -8 dBFS each tone	IMD3-9		(70)		dBc		4
Highest spur level (Dual-tone)							
4:1 MUX Fs = 6.4 GSps @ Fout1 = 2950 MHz, Fout2 = 2960 MHz -8 dBFS each tone	IMD3-9spur		(–90)		dBm		4
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @ 6.4 GSps			-30		dBm		4
Fc/2 @ 6.4 GSps			-85		dBm		4
Fc/4 @ 6.4 GSps			-80		dBm		4
Self-Noise Density at code 0 or 4095 @ 6.4 GSps			-147		dBm/Hz		4
Noise Power Ratio (1st Nyquist) –14 dBFS peak to rms loading factor Fs = 6.4 GSps 3.136 GHz broadband pattern, 64 MHz notch width	NPR		43		dB	(4) (5)	4

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level(1)
Equivalent ENOB (Computed from NPR figure)	ENOB		8.7		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		54.3		dB		4
Noise Power Ratio (1st Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps	NPR	47	50		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	9.3	9.8		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	58	61		dB		1, 6
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 6.4 GSps 3.136 GHz broadband pattern, 64 MHz notch width	NPR		38		dB		4
Equivalent ENOB (Computed from NPR figure)	ENOB		7.85		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		49		dB		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	41	43.5		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.3	8.8		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	52	54.5		dB		1, 6

Notes:

1. See Section 3.6 for explanation of test levels.
2. Refer to Figure 84 for SFDR variation versus temperature.
3. Refer to Figure 83 for SFDR variation versus supplies.
4. Refer to Figure 109 for NPR variation versus temperature.
5. Refer to Figure 108 for NPR variation versus supplies.

Table 6. AC Electrical Characteristics RTZ Mode (Second Nyquist Zone)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX Fs = 6.4 GSps @ Fout = 6336 MHz 0 dBFS Fs = 3.0 GSps @ Fout = 2970 MHz 0 dBFS	|SFDR|	 59	 48 64		 dBc	 (2) (3)	 4 1, 6
2:1 MUX Fs = 3.2 GSps @ Fout = 3168 MHz 0 dBFS Fs = 1.5 GSps @ Fout = 1485 MHz 0 dBFS	|SFDR|	 59	 59 66		 dBc	 (2) (3)	 4 1, 6
Highest spur level							
4:1 MUX Fs = 6.4 GSps @ Fout = 6336 MHz 0 dBFS Fs = 3.0 GSps @ Fout = 2970 MHz 0 dBFS			 –67 –74		 dBm		 4 1, 6
2:1 MUX Fs = 3.2 GSps @ Fout = 3168 MHz 0 dBFS Fs = 1.5 GSps @ Fout = 1485 MHz 0 dBFS			 –72 –75		 dBm		 4 1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @ 6.4 GSps			-27		dBm		4
Fc/2 @ 6.4 GSps			-84		dBm		4
Fc/4 @ 6.4 GSps			-80		dBm		4
Self-Noise Density at code 0 or 4095 @ 6.4 GSps			-137		dBm/Hz		4
Noise Power Ratio (2^{nd} Nyquist) –14 dBFS peak to rms loading factor Fs = 6.4 GSps 3.136 GHz broadband pattern, 64 MHz notch width	NPR		36		dB	(4) (5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		7.5		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		47		dB		4
Noise Power Ratio (2^{nd} Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	43.5	46		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.8	9.2		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	54.5	57		dB		1, 6

Notes:

1. See Section 3.6 for explanation of test levels.
2. Refer to Figure 84 for SFDR variation versus temperature.
3. Refer to Figure 83 for SFDR variation versus supplies.
4. Refer to Figure 109 for NPR variation versus temperature.
5. Refer to Figure 108 for NPR variation versus supplies.

Table 7. AC Electrical Characteristics RF Mode (Second to Ninth Nyquist Zones)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX							
Fs = 6.4 GSps @ Fout = 6336 MHz 0 dBFS			50				4
Fs = 6.4 GSps @ Fout = 9536 MHz 0 dBFS			50				4
Fs = 6.4 GSps @ Fout = 12736 MHz 0 dBFS			50				4
Fs = 6.4 GSps @ Fout = 19136 MHz 0 dBfs			43				4
Fs = 6.4 GSps @ Fout = 19264 MHz 0 dBFS	|SFDR|		44		dBc	(2) (3)	4
Fs = 6.4 GSps @ Fout = 25536 MHz 0 dBFS			44				4
Fs = 3.0 GSps @ Fout = 2970 MHz 0 dBFS		56	65				1, 6
Fs = 3.0 GSps @ Fout = 4470 MHz 0 dBFS		49	58				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 3168 MHz 0 dBFS			58				4
Fs = 3.2 GSps @ Fout = 4768 MHz 0 dBFS	|SFDR|		54		dBc	(2) (3)	4
Fs = 1.5 GSps @ Fout = 1485 MHz 0 dBFS		64	70				1, 6
Fs = 1.5 GSps @ Fout = 2235 MHz 0 dBFS		57	65			(6)	1, 6
4:1 MUX with IUCM2 Fs = 6.4 GSps @ Fout = 5940 MHz 0 dBFS	|SFDR|	54	58		dBc	(7)	1, 6
Highest spur level (Single tone)							
4:1 MUX							
Fs = 6.4 GSps @ Fout = 6336 MHz 0 dBFS			-66				4
Fs = 6.4 GSps @ Fout = 9536 MHz 0 dBFS			-70				4
Fs = 6.4 GSps @ Fout = 12736 MHz 0 dBFS			-73				4
Fs = 6.4 GSps @ Fout = 19136 MHz 0 dBFS			-75				4
Fs = 6.4 GSps @ Fout = 19264 MHz 0 dBFS			-75		dBm		4
Fs = 6.4 GSps @ Fout = 25536 MHz 0 dBFS			-77				4
Fs = 3.0 GSps @ Fout = 2970 MHz 0 dBFS			–69				1, 6
Fs = 3.0 GSps @ Fout = 4470 MHz 0 dBFS			–67				1, 6
2:1 MUX							
Fs = 3.2 GSps @ Fout = 1568 MHz 0 dBFS			–65				4
Fs = 3.2 GSps @ Fout = 4768 MHz 0 dBFS			–66		dBm		4
Fs = 1.5 GSps @ Fout = 1485 MHz 0 dBFS			–73				1, 6
Fs = 1.5 GSps @ Fout = 2235 MHz 0 dBFS			–75				1, 6
4:1 MUX with IUCM2 Fs = 6.0 GSps @ Fout = 5940 MHz 0 dBFS			–64		dBm	(7)	1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @ 6.4 GSps			-30		dBm		4
Fc/2 @ 6.4 GSps			-85		dBm		4
Fc/4 @ 6.4 GSps			-80		dBm		4
Dual-tone over Full Nyquist							

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
4:1 MUX Fs = 6.4 GSps @ Fout1 = 6150 MHz, Fout2 = 6160 MHz -8 dBFS each tone Fs = 6.4 GSps @ Fout1 = 9150 MHz, Fout2 = 9160 MHz -8 dBFS each tone Fs = 6.4 GSps @ Fout1 = 12550 MHz, Fout2 = 12560 MHz -8 dBFS each tone Fs = 6.4 GSps @ Fout1 = 15750 MHz, Fout2 = 15760 MHz -8 dBFS each tone	IMD3 IMD3 IMD3 IMD3		67 55 56 (48)		dBc		4 4 4 4
Highest spur level (Dual-tone)							
4:1 MUX Fs = 6.4 GSps @ Fout1 = 6150 MHz, Fout2 = 6160 MHz -8 dBFS each tone Fs = 6.4 GSps @ Fout1 = 9150 MHz, Fout2 = 9160 MHz -8 dBFS each tone Fs = 6.4 GSps @ Fout1 = 12550 MHz, Fout2 = 12560 MHz -8 dBFS each tone Fs = 6.4 GSps @ Fout1 = 15750 MHz, Fout2 = 15760 MHz -8 dBFS each tone	IMD3spur IMD3spur IMD3spur IMD3spur		-90 -80 -92 –91		dBm		4 4 4 4
Self-Noise Density at code 0 or 4095 @ 6.4 GSps			–133		dBm/Hz		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 6.4 GSps 3.136 GHz broadband pattern, 64 MHz notch width	NPR		35		dB	(4) (5)	4
Equivalent ENOB (Computed from NPR figure)	ENOB		7.4		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		46.2		dB		4
Noise Power Ratio (2nd Nyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	42.5	45		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.6	9.0		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	53.5	56		dB		1, 6
Noise Power Ratio (3rd Nyquist) –14 dBFS peak to rms loading factor Fs = 6.4 GSps 3.136 GHz broadband pattern, 64 MHz notch width	NPR		35.4		dB		4
Equivalent ENOB (Computed from NPR figure)	ENOB		7.4		Bit		4
Signal to Noise Ratio (Computed from NPR figure)	SNR		46.4		dB		4
Noise Power Ratio (3rdNyquist) –14 dBFS peak to rms loading factor Fs = 3 GSps 1.33 GHz broadband pattern, 17 MHz notch width	NPR	39	42		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	8.0	8.5		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	50	53		dB		1, 6

Table 8. AC Electrical Characteristics RF Mode (Second to Ninth Nyquist Zones) @ Fs=8.0 & 8.5 Gsps

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
Single-tone Spurious Free Dynamic Range							
4:1 MUX with IUCM2							
Fs = 8.0 GSps @ Fout = 8040 MHz 0 dBFS			54				4
Fs = 8.0 GSps @ Fout = 9400 MHz 0 dBFS	|SFDR|		48 (52)		dBc	(8)	4
Fs = 8.0 GSps @ Fout = 9960 MHz 0 dBFS			41			(9)	4
4:1 MUX with IUCM4							
Fs = 8.0 GSps @ Fout = 8020 MHz 0 dBFS		47	52 (58)				1, 6
Fs = 8.0 GSps @ Fout = 8700 MHz 0 dBFS	|SFDR|	40	45		dBc	(8)	1, 6
Fs = 8.0 GSps @ Fout = 8980 MHz 0 dBFS		40	43 (47)			(9)	1, 6
4:1 MUX with IUCM2							
Fs = 8.5 GSps @ Fout = 8542.5 MHz 0 dBFS			57				4
Fs = 8.5 GSps @ Fout = 9987.5 MHz 0 dBFS	|SFDR|		37 (42)		dBc	(8)	4
Fs = 8.5 GSps @ Fout = 10582.5 MHz 0 dBFS			42			(9)	4
4:1 MUX with IUCM4							
Fs = 8.5 GSps @ Fout = 8520 MHz 0 dBFS		40	52 (58)				1, 6
Fs = 8.5 GSps @ Fout = 9243 MHz 0 dBFS	|SFDR|	40	45		dBc	(8)	1, 6
Fs = 8.5 GSps @ Fout = 9542 MHz 0 dBFS		39	45 (48)			(9)	1,6
Highest spur level (Single tone)							
4:1 MUX with IUCM2							
Fs = 8.0 GSps @ Fout = 8040 MHz 0 dBFS			-74				4
Fs = 8.0 GSps @ Fout = 9400 MHz 0 dBFS			-62 (-66)		dBm	(8)	4
Fs = 8.0 GSps @ Fout = 9960 MHz 0 dBFS			-64			(9)	4
4:1 MUX with IUCM4							
Fs = 8.0 GSps @ Fout = 8020 MHz 0 dBFS			-63 (-76)				1, 6
Fs = 8.0 GSps @ Fout = 8700 MHz 0 dBFS			-60		dBm	(8)	1, 6
Fs = 8.0 GSps @ Fout = 8980 MHz 0 dBFS			-60 (-65)			(9)	1, 6
4:1 MUX with IUCM2							
Fs = 8.5 GSps @ Fout = 8542.5 MHz 0 dBFS			-72				4
Fs = 8.5 GSps @ Fout = 9987.5 MHz 0 dBFS			-58 (-66)		dBm	(8)	4
Fs = 8.5 GSps @ Fout = 10582.5 MHz 0 dBFS			-64			(9)	4
4:1 MUX with IUCM4							
Fs = 8.5 GSps @ Fout = 8520 MHz 0 dBFS			-61 (-73)				1, 6
Fs = 8.5 GSps @ Fout = 9243 MHz 0 dBFS			-60		dBm	(8)	1, 6
Fs = 8.5 GSps @ Fout = 9542 MHz 0 dBFS			-60 (-68)			(9)	1, 6
Signal independent Spur (clock-related spur) with 4:1 MUX							
Fc @ 8.0 GSps IUCM4			-30		dBm		4
Noise Power Ratio (9th Nyquist [8000M-9000M]) –14 dBFS peak to rms loading factor Fs = 8.0 GSps 980 MHz broadband pattern, 20 MHz notch width	NPR	30.5	36		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	6.6	7.5		Bit		1, 6
Signal to Noise Ratio (Computed from NPR figure)	SNR	41.5	47		dB		1, 6
Noise Power Ratio (9th Nyquist [8500M-9562.5M]) –14 dBFS peak to rms loading factor Fs = 8.5 GSps 1041.25 MHz broadband pattern, 21 MHz notch	NPR	29.5	34		dB		1, 6
Equivalent ENOB (Computed from NPR figure)	ENOB	6.43	7.2		Bit		1, 6

Parameter	Symbol	Min	Typ	Max	Unit	Notes	Test level (1)
Signal to Noise Ratio (Computed from NPR figure)	SNR	40.5	45		dB		1, 6

Notes:

1. See Section 3.6 for explanation of test levels.
2. Refer to Figure 84 for SFDR variation versus temperature.
3. Refer to Figure 83 for SFDR variation versus supplies.
4. Refer to Figure 109 for NPR variation versus temperature.
5. Refer to Figure 108 for NPR variation versus supplies.
6. This measurement at Fs = 1.5 GSps is done with RPB1 and RPW1.
7. The corresponding spectrum shows an output frequency at 5940 MHz within a 1500 MHz wide Nyquist zone.
8. See Section 5.6 Input Under Clocking Mode (IUCM)
9. For these measurements, test values without brackets are given with standard settings. Characterization values with brackets are given with optimized settings.

3.5 Timing Characteristics and Switching Performance

Unless otherwise specified:

Values in the table below are given over temperature range with typical power supplies (V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V), with 4:1 MUX ratio, typical swing on input data, typical Pclk, master clock input jitter is below 100 fs rms integrated over 11 GHz bandwidth.

Min and Max values are given over temperature range.

Typ values are given at ambient temperature.

Table 9. Timing characteristics and Switching Performance

Parameter	Symbol	Value	Unit	Note	Test Level (1)
SWITCHING PERFORMANCE AND CHARACTERISTICS					
Maximum operating clock frequency					
4:1 MUX mode IUCM4 or IUCM2		8.5	GHz		4
4:1 MUX mode IUCM1		6.4	GHz		4
2:1 MUX mode		3.2	GHz		4
Minimum operating clock frequency		300	MHz	(2)	5

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test Level (1)
TIMING CHARACTERISTICS							
Input Data timing							
Input data setup and hold time	t_{SH}		320		ps	(3)	4
Input data rate (4:1 MUX) IUCM2				1062.5	Msps		4
Input data rate (4:1 MUX) IUCM4				531.25	Msps		4
Input data rate (4:1 MUX)				1600	Msps		4
Input data rate (2:1 MUX)				1600	Msps		4
Data clock output timing (DSP, DSPN)							
DSP clock phase tuning steps	PSS		0.5		Tclock		5
Master clock to DSP timing							
Pipeline (4:1 MUX)			3		Tclock	(4)	5
Pipeline (2:1 MUX)			3				5
Delay 4:1 MUX	t_{PD}		540		ps		4
Delay 2:1 MUX			540				4
SYNC to DSP, DSPN							
Sync falling edge to DSP rising edge Pipeline in 4:1 MUX			3		Tclock	(5)	5
Sync falling edge to DSP rising edge Pipeline in 2:1 MUX			3		Tclock		5
Sync falling edge to DSP rising edge Delay with 2:1 MUX	t_{SDSP}		640		ps		4
Delay with 4:1 MUX			640		ps		4
Sync rising edge to DSP falling edge	t_{SDSPF}		T_{CLK} + 1/2 T_{DSP}		ps		5

Parameter	Symbol	Min	Typ	Max	Unit	Note	Test Level(1)
SYNC timing							
Minimum Sync pulse width			3		Tclock		4
SYNC setup and hold time	t_{SSH}		15		ps	(6)	4
SYNC forbidden area lower bound	t_1		100		ps		4
SYNC forbidden area upper bound	t_2		$t_1 - t_{SSH}$		ps		4
Analog output timing							
Analog output rise time (20-80%)	t_{OR}		30		ps		4
Analog output fall time (20-80%)	t_{OF}		30		ps		4
Pipeline (4:1 MUX)			3		Tclock	(4)	5
Pipeline (2:1 MUX)			3				5
Analog output delay	t_{OD}		560		ps	(4)	4

Notes:

1. See Section 3.6 for explanation of test levels.
2. Minimum operating clock frequency can be DC. It depends on the clock input AC coupling capacitor used in the final application and limitation due to the environment as circuit itself displays no lower clock frequency limitation.
3. Set up and hold time were measured on Teledyne e2v evaluation board and as such include the impact from FPGA (jitter and skew) and PCB skew on the board. Refer to Figure 121 on Section 7.3 t_{SH} variation over temperature range is around 20 ps.
4. See Figure 2 and Figure 3 below
5. See Figure 6 below.
6. See Figure 7 below.

Figure 2. Timing Diagram for 4:1 MUX principle of operation OCDS1, IUCM1

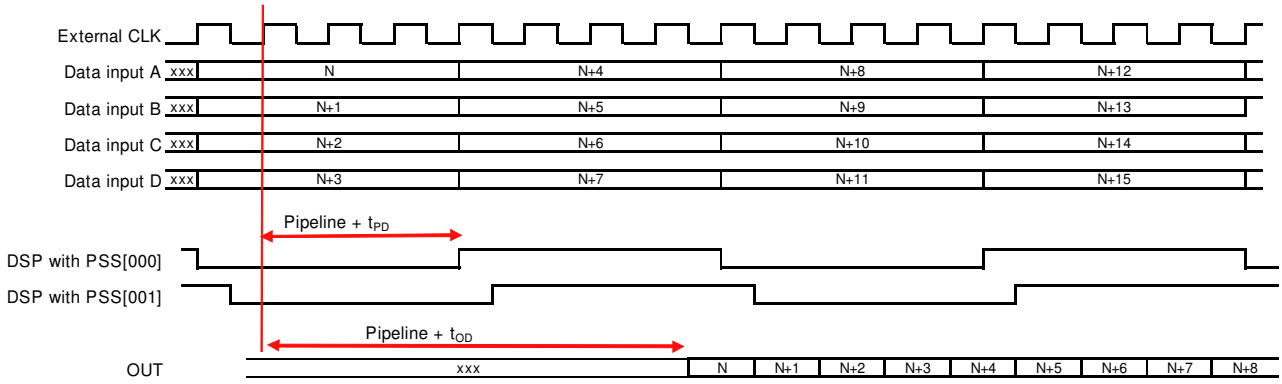


Figure 3. Timing diagram for 4:1 MUX principle of operation, IUCM2

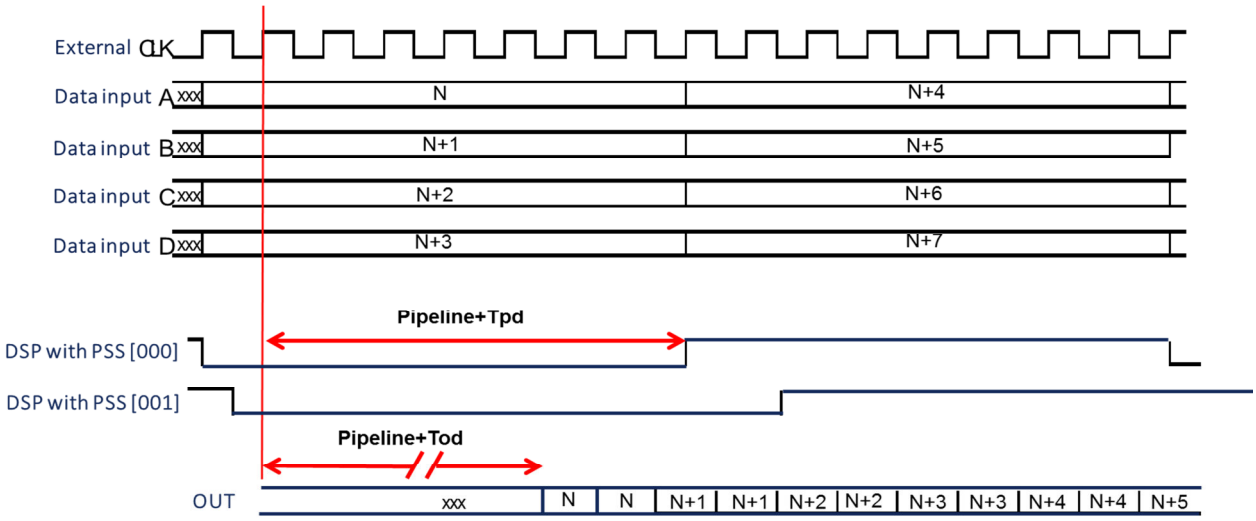


Figure 4. Timing Diagram for 4:1 MUX principle of operation OCDS1, IUCM4

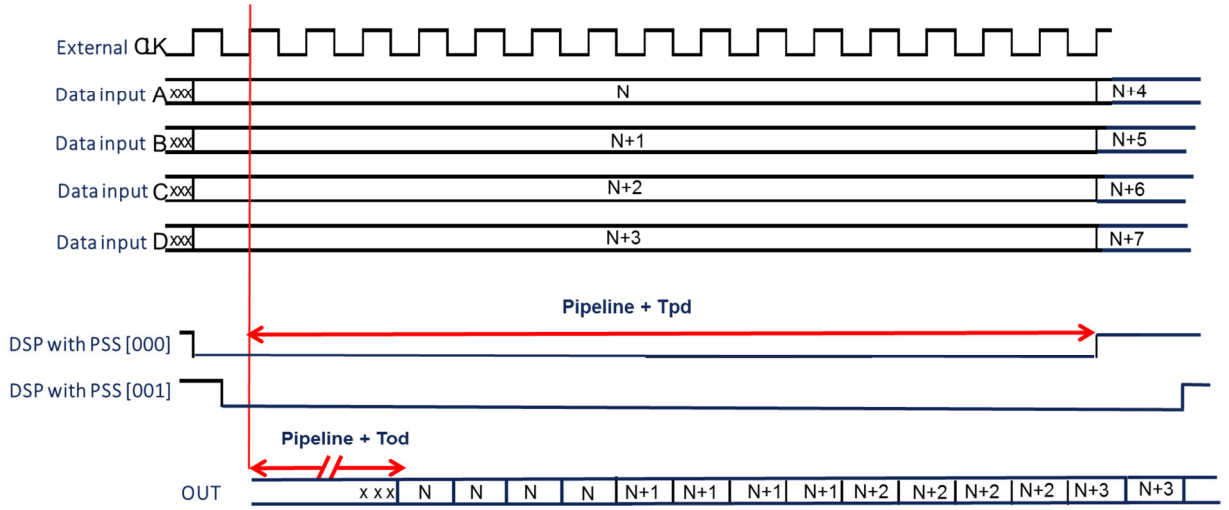


Figure 5. Timing Diagram for 2:1 MUX principle of operation OCDS1, IUCM1

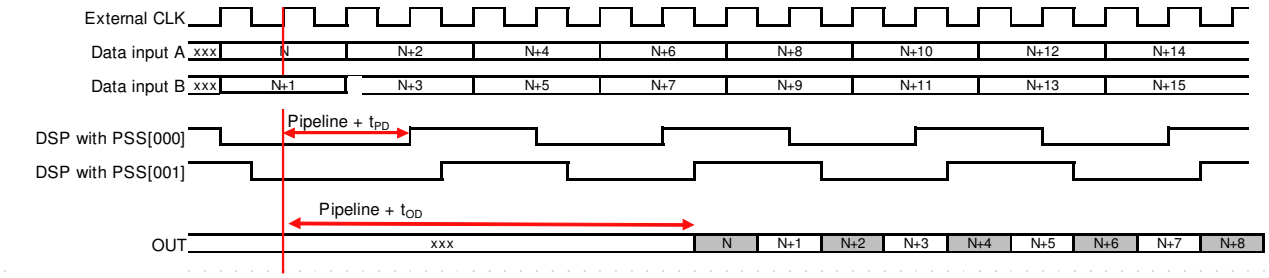


Figure 6. Timing relationship between SYNC and DSP

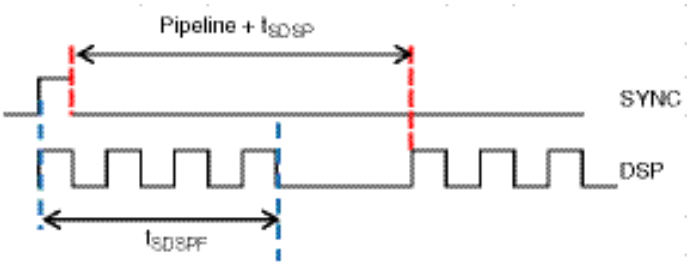
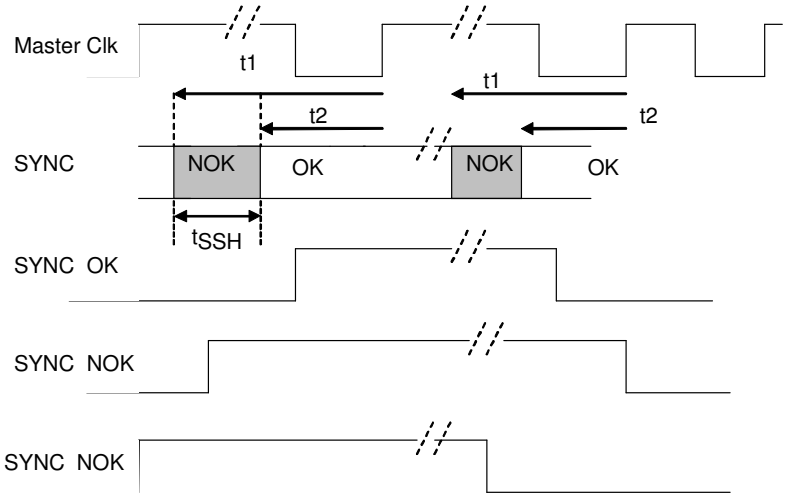


Figure 7. SYNC Timing Diagram



3.6 Explanation of Test Levels

Table 10. Test levels

1	100% production tested at +25°C[1]
2	100% production tested at +25°C[1], and sample tested at specified temperatures.
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is only guaranteed by design
6	100% tested over specified temperature range (-55°C<TC, Tj<125°C)

Only MIN and MAX values are guaranteed.

Note: 1. Unless otherwise specified.

3.7 Digital Input Coding Table

Table 11. Coding Table (Theorical values)

Digital output msb……..lsb	**Differential analog output**
000000000000	–500 mV
010000000000	–250 mV
011000000000	–125 mV
011111111111	–0.122 mV
100000000000	0.122 mV
101000000000	+125 mV
110000000000	+250 mV
111111111111	+500 mV

4 DEFINITION OF TERMS

Table 12. Definition of Terms

Abbreviation	Term	Definition
(SFDR)	Spurious free dynamic range	Ratio expressed in dBC of the signal power, set at Full Scale, to the power of the highest spurious spectral component over the Nyquist zone. The peak spurious component may or may not be a harmonic.
(HSL)	Highest Spur Level	Power of the highest spurious spectral component expressed in dBm.
(ENOB)	Effective Number Of Bits	ENOB is calculated from NPR measurement using the formula: ENOB = ($NPR_{[dB]}$ + $\|LF_{[dB]}\|$ 3 - 1.76) / 6.02 Where LF is the loading factor i.e. the ratio between the Gaussian noise standard deviation versus amplitude full scale of the NPR pattern.
(SNR)	Signal to noise ratio	SNR is calculated from NPR measurement using the formula: $SNR_{[dB]} = NPR_{[dB]} + \|LF_{[dB]}\| - 3$ Where LF is the loading factor i.e. the ratio between the Gaussian noise standard deviation versus amplitude full scale of the NPR pattern.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the DAC performance in response to broad band signals. When applying a notch-filtered broadband white-noise pattern at the input of the DAC under test, the Noise Power Ratio is defined as the ratio between the average noise measured on the shoulder of the notch and inside the notch, using the same integration bandwidth.
(DNL)	Differential non linearity	The Differential Non Linearity for a given code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there is no missing point and that the transfer function is monotonic.
(INL)	Integral non linearity	The Integral Non Linearity for a given code i is the difference between the measured voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the insertion loss linked to the power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (i.e. 99% power transmitted and 1% reflected).
(IUCM)	Input Under Clocking Mode	The IUCM principle is to apply a selectable division ratio between the DAC clock section and the MUX clock section.
(PSS)	Phase Shift Select	The Phase Shift Select function is used to tune the phase of the DSP clock.
(OCDS)	Output Clock Division Select	It allows dividing the DSP clock frequency by the OCDS coded value factor.
(NRZ)	Non Return to Zero	Non Return to Zero mode on analog output.
(RF)	Radio Frequency	RF mode on analog output.
(RTZ)	Return To Zero	Return to zero mode on analog output.
(NRTZ)	Narrow Return To Zero	Narrow return to zero mode on analog output.
(RPB)	Reshaped Pulse Begin	Function controlling when the transition of the DAC analog output occurs. (applicable in NRTZ, RTZ and RF mode)
(RPW)	Reshaped Pulse Width	Function controlling the width of the reshaping of the DAC analog output. (applicable in NRTZ and RF mode)
(MDA)		Mux delay adjust

5 FUNCTIONAL DESCRIPTION

Figure 8. DAC functional diagram

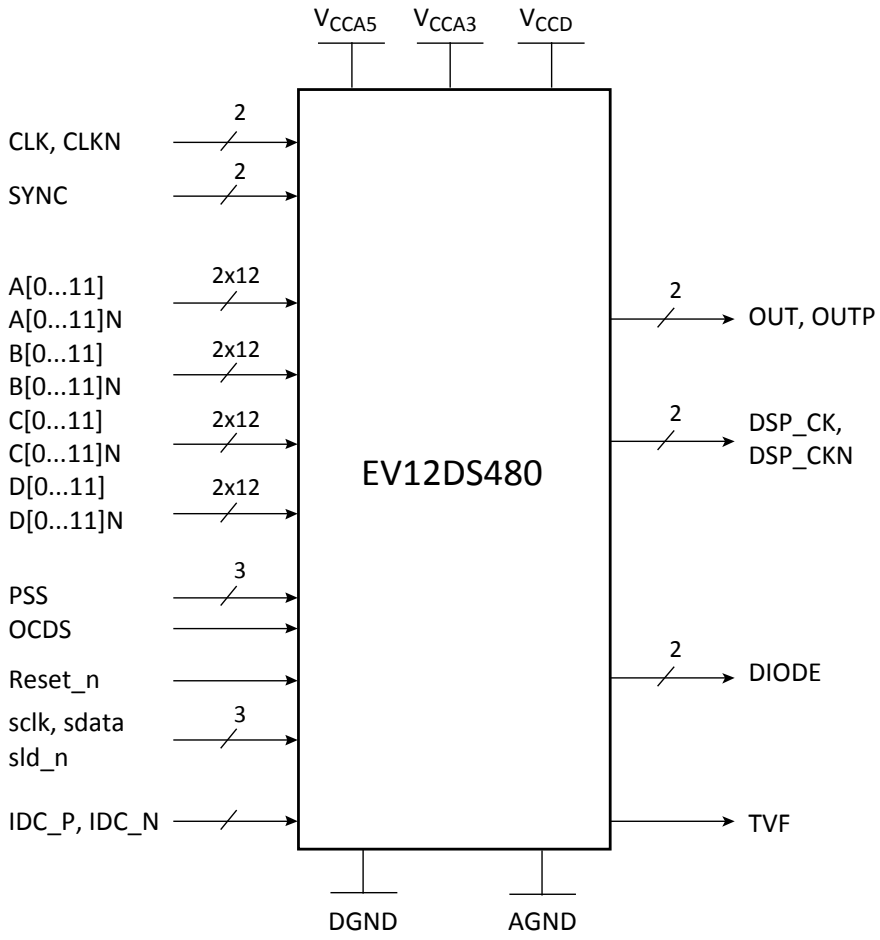


Table 13. Functions description

Name	Function	Name	Function
V_{CCD}	3.3V digital power supply	CLK	In-phase master clock
V_{CCA5}	5V analog power supply	CLKN	Inverted phase master clock
V_{CCA3}	3.3V analog power supply	DSP_CK	In-phase output clock
DGND	Digital ground	DSP_CKN	Inverted phase output clock
AGND	Analog ground	PSS[0..2]	Phase shift select
A[11…0]	In-phase digital input port A	Reset_n	Reset of 3WSI registers
A[11..0]N	Inverted phase digital input port A	sld_n	3WSI select
B[11…0]	In-phase digital input port B	sclk, sdata	3WSI clock and data inputs
B[11..0]N	Inverted phase digital input port B	TVF	Setup/hold time violation flag
C[11…0]	In-phase digital input port C	IDC_P, IDC_N	Input data check
C[11..0]N	Inverted phase digital input port C	OCDS	Output Clock Division factor Selection
D[11…0]	In-phase digital input port D	Diode	Diode for temperature monitoring
D[11..0]N	Inverted phase digital input port D	SYNC/ SYNCN	Synchronization signal (active high)
OUT	In-phase analog output	OUTN	Inverted phase analog output

Table 14. DAC overview functionality and controls

Function	Description	Controllability
MUX	MUX ratio selection (4:1 or 2:1)	3WSI
MODE	Output reshaping mode selection: NRZ, NRTZ, RTZ or RF	3WSI
RPW	Reshaping Pulse Width (applicable in NRTZ and RF mode)	3WSI
RPB	Reshaping Pulse Begin (applicable in NRTZ, RTZ and RF mode)	3WSI
PSS	Phase Shift Select: shift the DSP clock by steps of $T_{CLK}/2$ for FPGA synchronization	3WSI/external pins
OCDS	Output Clock Division Select: Ratio of division between DSP clock and master clock	3WSI/external pins
IUCM	Internal Under Clocking Mode ratio selection: Allow to work with data rate equal to F_{CLK} divided by 1,2 or 4 with a DAC clocked at F_{CLK}	3WSI
GA	DAC Gain Adjust	3WSI
MDA	Mux delay adjust used in IUCM2 & 4 mode at 8.0 Gsps & 8.5 Gsps	3WSI

Note:

1. PSS and OCDS are controlled through the external pin if ECDC bit of 3WSI state register is set to level 1 (default value). See Section 5.14.3 or more information.

5.1 Multiplexer

Two multiplexer ratios (N) are allowed:

- N = 4: 4:1 MUX, which allows operation up to 8.5GSps;
- N = 2: 2:1 MUX, which allows operation up to 3.2 GSps.

Label	Value	Description	Default setting
MUX	0	4:1 mode (N = 4)	0 (4:1MUX mode)
	1	2:1 mode (N = 2)	

In 2:1 MUX ratio, the unused data ports (ports C and D) can be left open.

5.2 Mode Function

The MODE function allows choosing between NRZ, NRTZ, RTZ and RF modes.

Label	Value	Description	Default setting
MODE[1:0]	00	NRZ mode	01 (NRTZ)
	01	Narrow RTZ (a.k.a. NRTZ) mode	
	10	RTZ Mode (50%)	
	11	RF mode	

Ideal equations describing maximum available output power versus analog output frequency in the four modes are given hereafter, with X being the normalised output frequency (i.e. Fout/F_{CLK}, thus the edges of the Nyquist zones are at X = 0, ½, 1, 3/2, 2, …).

In fact, due to limited bandwidth, an extra term must be added to take into account a first order low pass filter with a 7.5 GHz cut-off frequency.

In the following formula, Pout (X) is expressed in dBm. (Hence 0.893 in formula converting the dB to dBm)

NRZ mode:

$$\mathrm{Pout}(X) = 20.\log_{10}.\frac{k.\ \mathrm{sinc}(k.\ \pi.X)}{0.893}$$

where sinc(x) = sin(x)/x, and k = 1

NRTZ mode:

$$\mathrm{Pout(X)} = 20.\log_{10}.\frac{\mathrm{k}.\ \mathrm{sinc(k.\ \pi.X)}}{0.893}$$

where k = 1 - RPW/T_{CLK} and RPW is the width of reshaping pulse

RTZ mode:

$$\mathrm{Pout(X)} = 20.\log_{10}.\frac{\mathrm{k}.\ \mathrm{sinc(k.\ \pi.X)}}{0.893}$$

where k is the duty cycle of the clock presented at the DAC input. Please note that due to phase mismatch in balun used to convert single ended clock to differential clock the first zero may move around the limit of the 4th and the 5th Nyquist zone. Ideally k = 1/2.

RF mode:

$$\mathrm{Pout(X)} = 20.\log_{10}.\frac{\mathrm{k}.\ \mathrm{sinc}\left(\frac{\mathrm{k.\ \pi.X}}{2}\right).\sin\left(\frac{\mathrm{k.\ \pi.X}}{2}\right)}{0.893}$$

where k = 1 - RPW/T_{CLK} and RPW is the width of reshaping pulse. As a consequence:

- NRZ mode offers maximum output power for 1st Nyquist operation;
- RTZ mode have a slow roll off for 2nd Nyquist operation;
- RF mode offers maximum power over 2nd and 3rd Nyquist zones;
- NRTZ mode offers optimum power over the 1st and the first half of the 2nd Nyquist zones. It is the most relevant mode in terms of performance for operation over 1st and beginning of 2nd Nyquist zones.

In the two following Figure 9. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 6.4 GSps in IUCM1, over four Nyquist zones, computed for different RPW steps and Figure 10. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 3.2 GSps, over eight Nyquist zones, computed for different RPW steps, the pink line is the ideal equation's result, and the green line includes a first order 7.5 GHz cut-off low pass filter to take into account the bandwidth effect due to die and package.

Figure 9. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 6.4 GSps in IUCM1, over four Nyquist zones, computed for different RPW steps

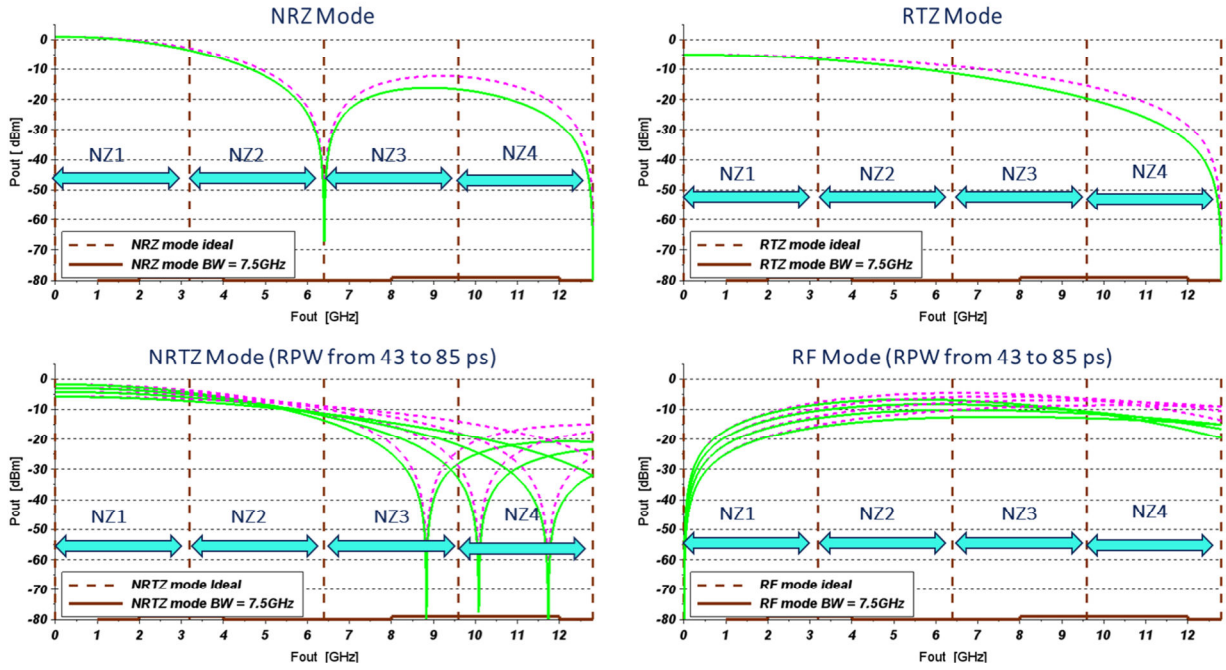
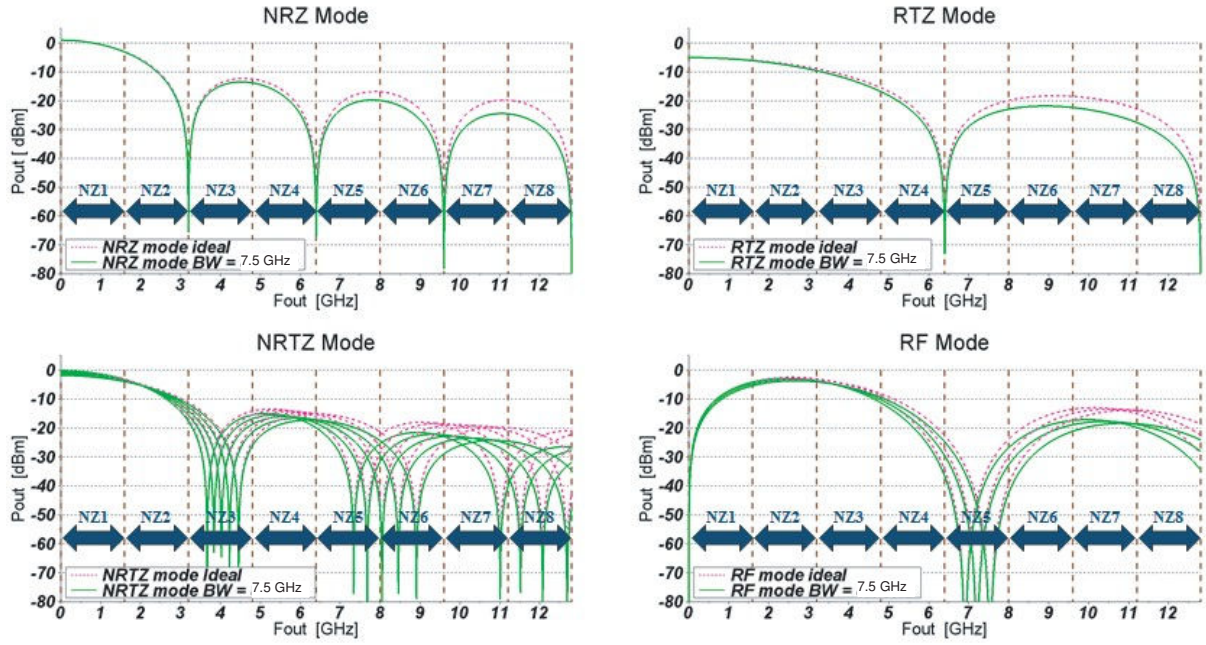


Figure 10. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 3.2 GSps, over eight Nyquist zones, computed for different RPW steps



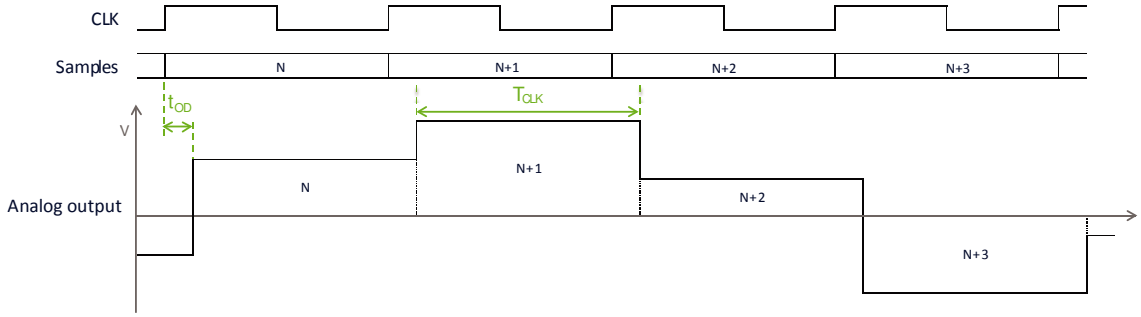
5.2.1 NRZ output mode

This mode does not allow for operation in the 2nd Nyquist zone because of the sin(x)/x notch.

The advantage is that it gives good results at the beginning of the 1st Nyquist zone (less attenuation than in RTZ mode); it also removes the parasitic spur at the clock frequency (in differential).

This legacy mode provides the highest output power at the beginning of the 1st Nyquist zone.

Figure 11. NRZ timing diagram

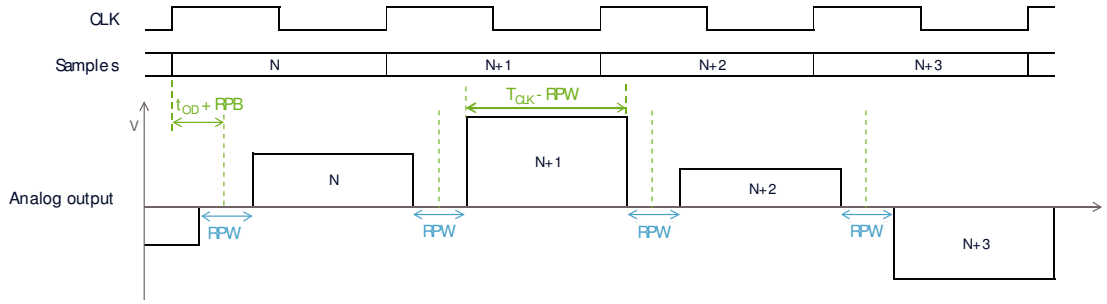


5.2.2 Narrow RTZ (NRTZ) output mode

This mode has the following advantages:

- Optimized power in the 1st Nyquist zone and beginning of the 2nd Nyquist zone;
- Extended dynamic and linearity through elimination of noise on transition edges;
- Trade-off between NRZ and RTZ;
- Possible operation in the 4th and 5th Nyquist zones. And weaknesses:
- Notch in the 3rd Nyquist zone. In fact, notches are at N*(1/(T_{CLK} - RPW)), where T_{CLK} is the external clock period and RPW is the reshaping pulse width;
- By construction clock spur at F_{CLK}.

Figure 12. Narrow RTZ timing diagram



The RPB and RPW settings are applicable in this mode; they are programmable through the 3 wire serial interface. For more information on RPB and RPW see Section 5.3.

5.2.3 RTZ output Mode

The advantage of the RTZ mode is that it enables the operation in the 2nd Nyquist zone but the drawback is that it attenuates more the signal in the first Nyquist zone.

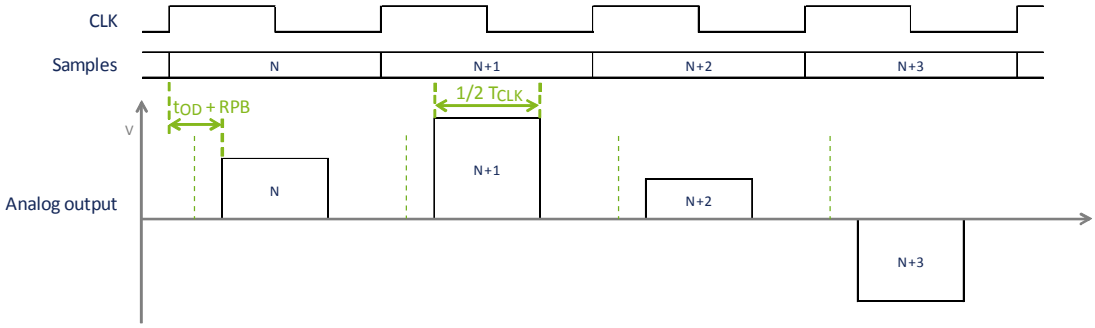
Advantages:

- Extended roll off of sin(x)/x;
- Extended dynamic and linearity through elimination of noise on transition edges;

Weakness:

- By construction strong clock spur at F_{CLK}.

Figure 13. RTZ timing diagram



The RPB setting is applicable in this mode; it is programmable through the 3 wires serial interface. For more information on RPB see Section 5.3.

5.2.4 RF output mode

RF mode is optimal for operation at high output frequency, since the decay with frequency occurs at higher frequency than for RTZ. Unlike NRZ or RTZ modes, the RF mode presents notches at DC and $2N*(1/(T_{CLK} - RPW)$, and minimum attenuation for Fout = $1/(T_{CLK} - RPW)$.

Its principle is that the output is at its value during half the sampling period and at its opposite value during the remaining half.

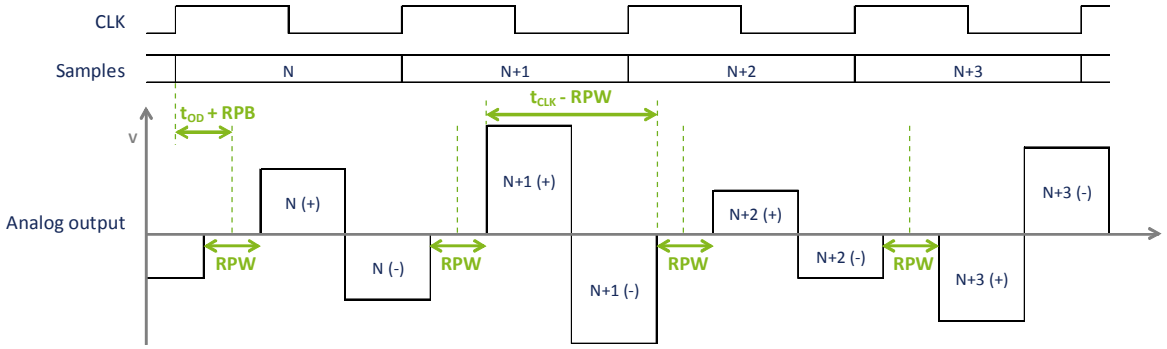
Advantages:

- Optimized for operations over the second half of the 2nd Nyquist zone or over the 3rd Nyquist zone in IUCM1;
- Extended dynamic and linearity through elimination of noise on transition edges;
- Possible operation proven in the first half of the 4th Nyquist zone.
- Used in IUCM2 (4th and 5th Nyquist zone) and IUCM4 (8th and 9th Nyquist zone)

Weakness:

- By construction clock spur at F_{CLK}.
- Next clock spur pushed to $2.F_{CLK}$.

Figure 14. RF timing diagram



RPB and RPW settings are applicable in this mode; they are programmable through the 3 wire serial interface. For more information on RPB and RPW see Section 5.3.

5.3 RPW and RPB Feature

RPB (Reshaping Pulse Begin) and RPW (Reshaping Pulse Width) are new features of the EV12DS480A. They can be used to fine tune the performance of the different modes of the DAC. Their objective is to control the rejection of the signal transitions.

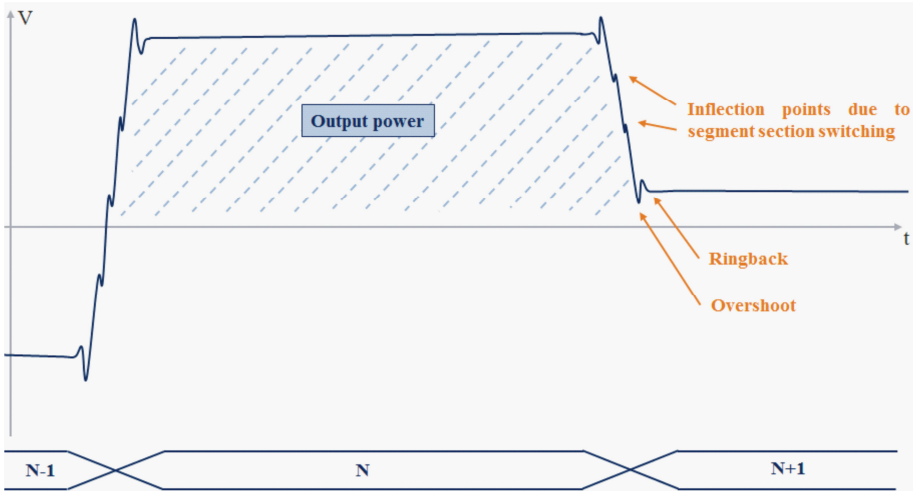
These 2 settings are controlled via the 3WSI interface. See Section 5.3 for more information on the 3WSI interface. The different values they can take are specified by mode in the following paragraphs.

Note: In the following figures, the perturbation on the analog output in time domain has been exacerbated to facilitate the comprehension.

NRZ Mode:

See below the output of the DAC in NRZ mode in time domain:

Figure 15. DAC output in NRZ and time domain



As can be seen above, in NRZ mode, the transition contains a lot of perturbations that translates into harmonics in the spectrum. However the output power is maximum. RPB or RPW settings are not available in this mode.

RTZ Mode:

In RTZ mode, the output is on 50% of the sampling period and off the remaining 50% of the sampling period. Per definition of the RTZ mode, its output power is half the one of the NRZ output power. In this mode, the DAC features the RPB function which controls when the transition between 50% on and 50% off occurs. Using this feature, the RTZ output linearity performance can be increased. See below the output of the DAC in RTZ mode and time domain, whether RPB is correctly configured or not (the NRZ output mode is traced to show the difference between NRZ and RTZ mode):

Figure 16. DAC output in RTZ mode and time domain when RPB is optimum

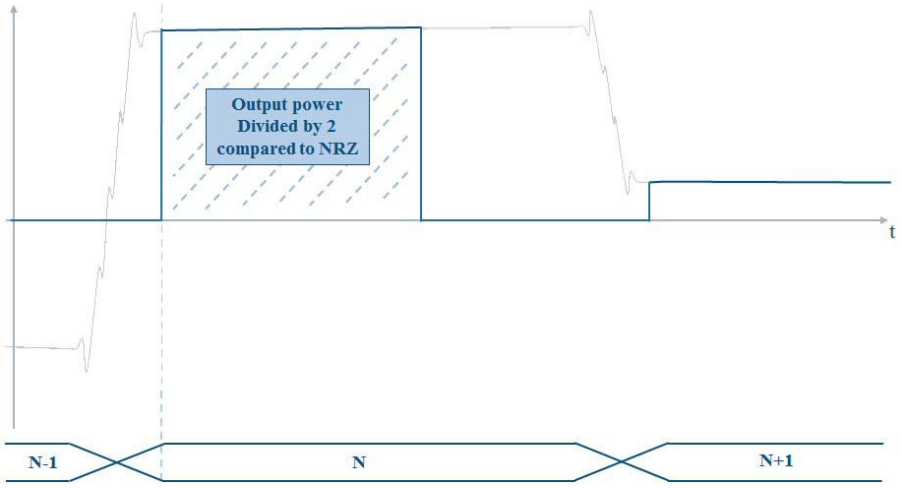
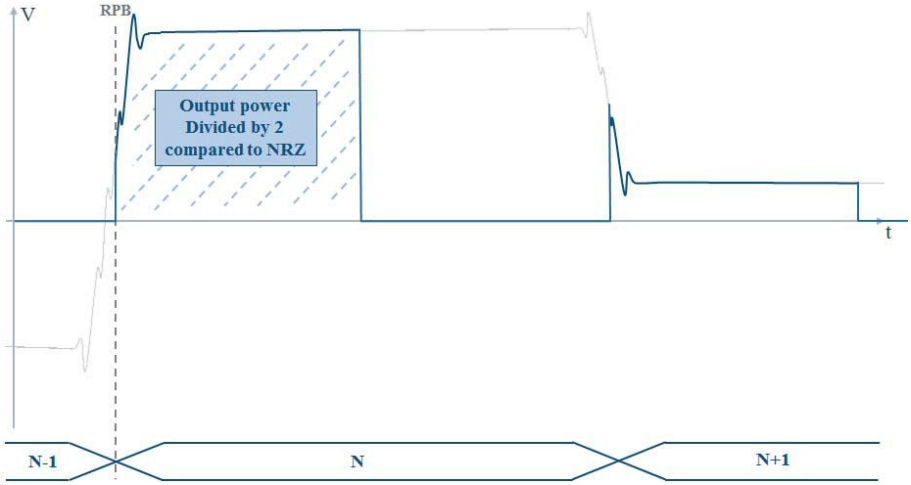


Figure 17. DAC output in RTZ mode and time domain when RPB is not optimum



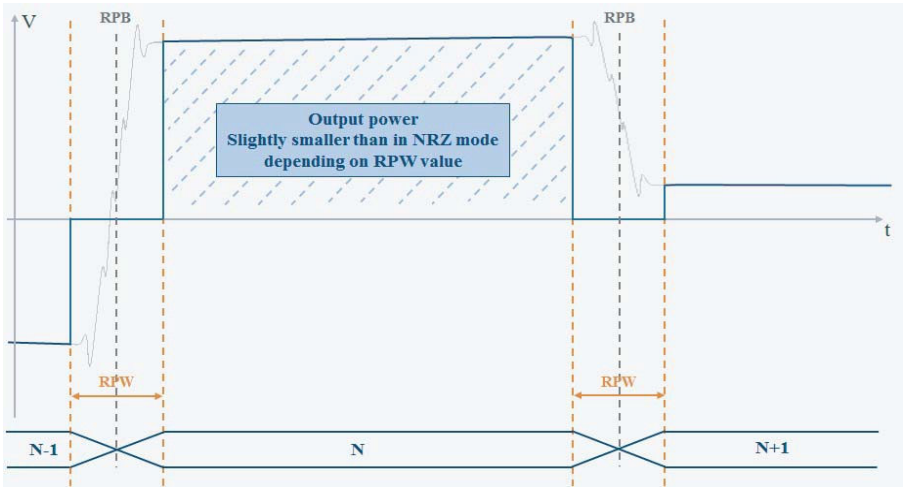
Tuning RPB as depicted in Figure 5-9 will improve the linearity of the output because the transition will be completely rejected. If RPB is not tuned to reject the transitions (see Figure 5-10), the output harmonics will be degraded (mainly H3).

The RPW setting is not available in RTZ mode. See Section 5.14.3 for the available values for RPB in RTZ mode.

NRTZ Mode:

The NRTZ mode is a compromise between the NRZ and the RTZ modes. Its objective is to have the best possible linearity through the removal of the transitions while keeping a high output power. Thus, only the transitions should be cancelled. In this mode both RPB and RPW settings are available. The RPB setting controls the position where the signal is cancelled. The RPW setting controls the wideness of the cancelled signal. See below an example where RPB and RPW are optimum in NRTZ mode (the NRZ output mode is traced to show the difference between NRZ and NRTZ mode):

Figure 18. DAC output in NRTZ mode and time domain when RPB/RPW are optimum



In the case above, the output has a better linearity than in NRZ mode over the complete spectrum while suffering from a slight output power reduction.

Figure 19. DAC output in NRTZ mode and time domain when RPB is not optimum

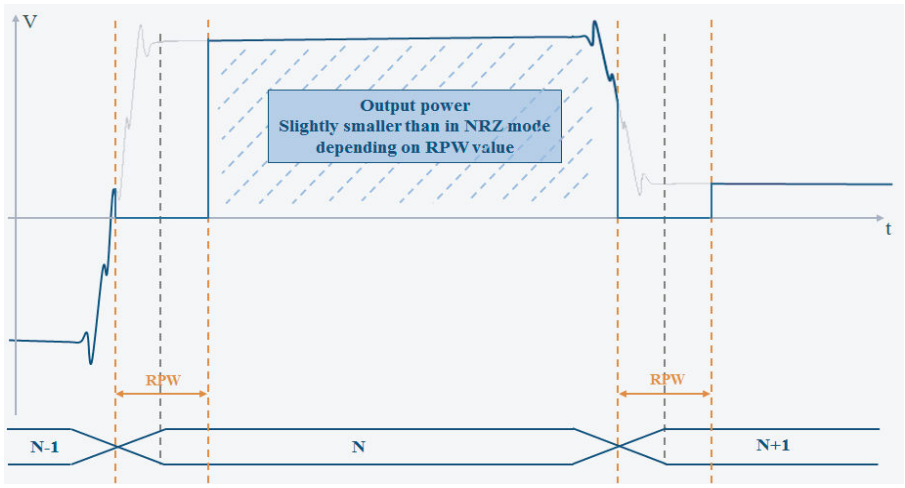
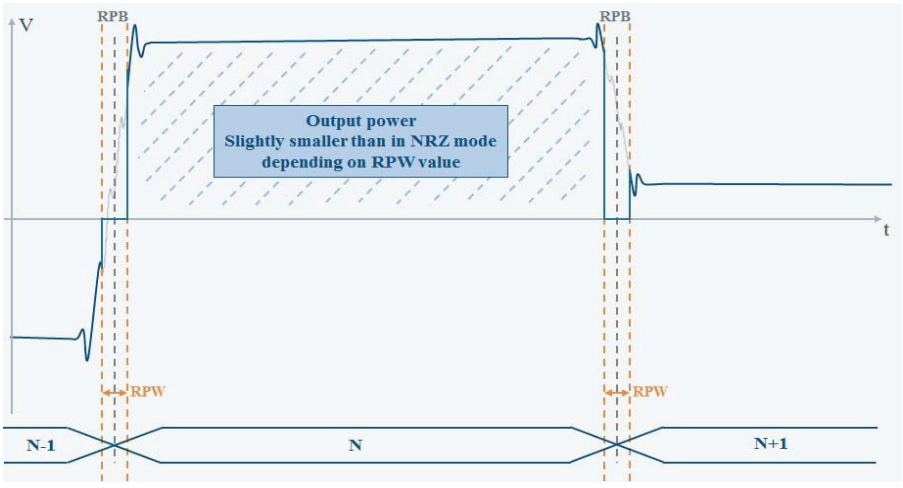


Figure 20. DAC output in NRTZ mode and time domain when RPW is not optimum



In case RPB is not optimum (Figure 5-12), the harmonics will be degraded (mainly H3). In case RPW is smaller than the optimum (Figure 5-13), the linearity of the output will be degraded. In case RPW is larger than the optimum, the DAC will have high linearity performance but lower output power.

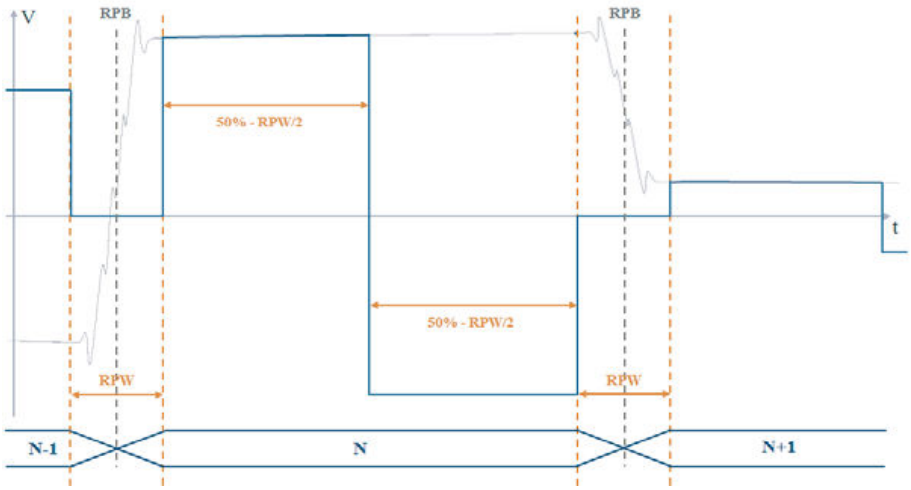
The RPW setting impacts the frequency response of the mode. See below the Pout vs Fout figure in NRTZ mode with different RPW values:

See Section 5.14.3 for the available values for RPB and RPW in NRTZ mode.

RF Mode:

To improve linearity of this mode both RPB and RPW settings are available. See below an example where RPB and RPW are optimum in RF mode (the NRZ output mode is traced in light color to show the difference between NRZ and RF mode):

Figure 21. DAC output in RF mode and time domain when RPB and RPW are optimum



In case RPB is not optimum, the harmonics will be degraded (mainly H3). In case RPW is smaller than the optimum, the linearity of the output will be degraded. In case RPW is larger than the optimum, the DAC will have high linearity performance but lower output power.

The RPW setting impacts the frequency response of the mode. See Section 6.2.1.

See Section 5.14.3 for the available values for RPB and RPW in RF mode.

5.4 Phase Shift Select function (PSS)

It is possible to adjust the timing between the sampling clock and the output DSP clock.

The DSP clock output phase can be tuned over a range of 3.5 input clock cycles (7 steps of half a clock cycle) in addition to the intrinsic propagation delay between the DSP clock (DSP, DSPN) and the sampling clock (CLK, CLKN).

Three bits are provided for the phase shift function: PSS[2:0].

By setting these 3 bits to 0 or 1, one can add a delay on the DSP clock in order to properly synchronize the input data of the DAC and the sampling clock (the DSP clock should be applied to the FPGA and should be used to clock the DAC digital input data).

These 3 bits are either driven directly through the pins PSS[2:0] or through the 3WSI depending on the ECDC bit in the state register of the 3WSI.

Table 15. PSS coding table

Label	Value	Description
PSS[2:0]	000	No additional delay on DSP clock (Default value)
	001	0.5 input clock cycle delay on DSP clock
	010	1 input clock cycle delay on DSP clock
	011	1.5 input clock cycle delay on DSP clock
	100	2 input clock cycles delay on DSP clock
	101	2.5 input clock cycles delay on DSP clock
	110	3 input clock cycles delay on DSP clock
	111	3.5 input clock cycles delay on DSP clock

In order to determine how much delay needs to be added on the DSP clock to ensure the synchronization between the input data and the sampling clock within the DAC, the TVF bit should be monitored.

Note: In 4:1 MUX mode the 8 settings are relevant, in 2:1 MUX only the four first settings are relevant; the four last settings will yield the same results.

Figure 22. PSS timing diagram for 4:1 MUX, OCDS = 0

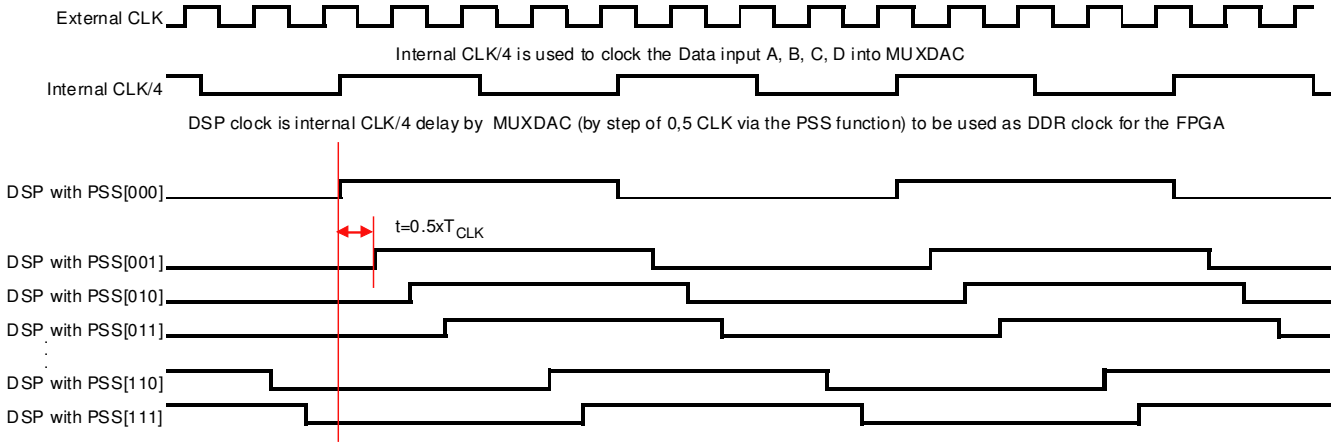
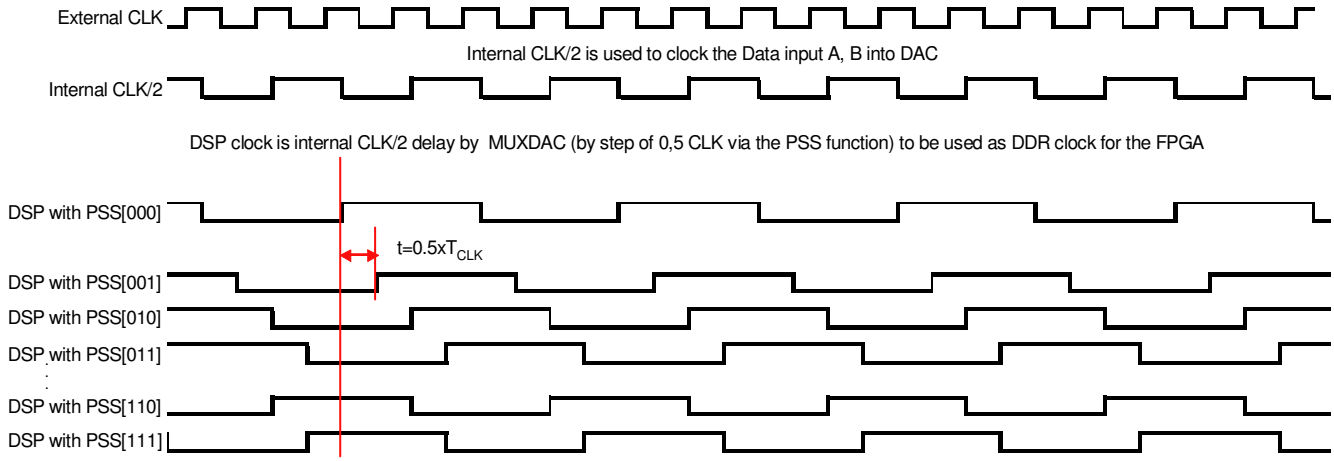


Figure 23. PSS timing diagram for 2:1 MUX, OCDS = 0



5.5 Output Clock Division Select function (OCDS)

It is possible to change the DSP clock internal division factor from 1 to 2 with respect to the sampling clock/(2*N*M) where N is the MUX ratio (2 or 4), and M is the IUCM ratio (1, 2 or 4). This is possible via the OCDS Output Clock Division Select bit through the 3WSI or the external pins if the ECDC bit is high.

OCDS is used to obtain a synchronization clock for the FPGA slow enough to allow the FPGA to operate with no further internal division of this clock, thus its internal phase is determined by the DSP clock phase. This is useful in a system with multiple DACs and multiple FPGAs to guarantee deterministic phase relationship more easily between the FPGAs after a synchronization of all the DACs.

Table 16. OCDS coding table

Label	Value	Description	Default setting
OCDS	0	OCDS1: DSP clock = Sampling Clock/(2*N*M)	0 (OCDS1)
	1	OCDS2: DSP clock = Sampling Clock/(2*N*M*2)	

Figure 24. OCDS timing diagram for 4:1 MUX and IUCM1 mode

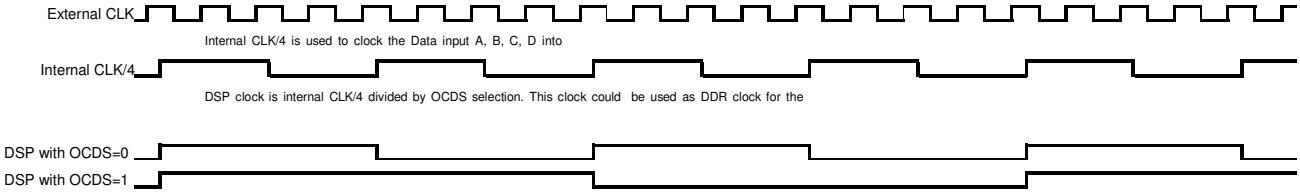
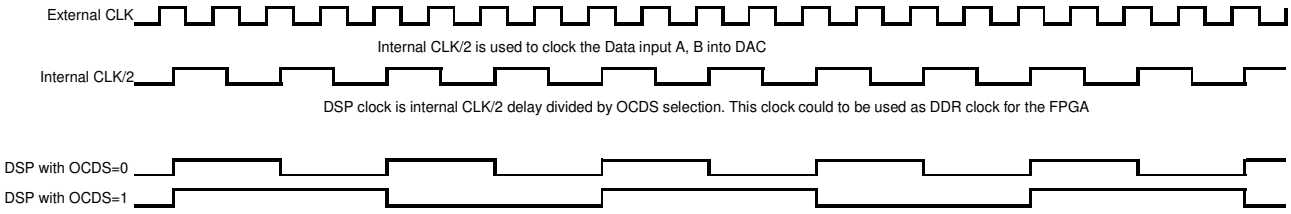


Figure 25. OCDS timing diagram for 2:1 MUX and IUCM1 mode



5.6 Input Under Clocking Mode (IUCM)

Three Input Under Clocking Mode (IUCM) settings are available for both 4:1 MUX and 2:1 MUX modes, selectable through the 3WSI (see 3WSI description).

The principle is to apply a division ratio (1, 2 or 4) between the DAC clock section and the MUX clock section:

- IUCM1: MUX is driven by the same clock than the DAC section (default mode).
- IUCM2: MUX is driven by a divided by 2 clock coming from the DAC section
- IUCM4: MUX is driven by a divided by 4 clock coming from the DAC section

Compared to the default mode, using IUCM2 or IUCM4 then reduces the input data rate by the same factor with a same sampling rate. As a result, a data will be sampled 2 or 4 times respectively.

See Figure 3 and Figure 4

Using IUCM2 or 4 settings allows operating the DAC up to 8.5 GSps. As a result, the benefit of using the IUCM2 or 4 is to reach higher output power levels thanks to the higher sampling rate on the Nyquist zones adjacent to the Fclock (see spectral response below) together with lower requirements on the LVDS input data rate. The drawback is a decrease of the Nyquist Zone width by the same factor than the IUCM value.

Theoretical Pout curves in RF mode, at 8Gsps, IUCM1, IUCM2, IUCM4 are shown below.
IUCM1 at 8.0 Gsps curve is given for reference only and cannot be used due to FPGA output data rate limitation (The maximum sampling rate in IUCM1 is 7Gsps).
The Nyquist zones are shown for IUCM4 and IUCM2. In IUCM4, the NZ8 and NZ9 Nyquist zones can be used.
In IUCM2, the NZ4 and NZ5 Nyquist zones can be used.

Figure 26. Pout curves in RF mode at 8.0 GSps from DC to 12 GHz in IUCM1, IUCM2 and IUCM4 modes

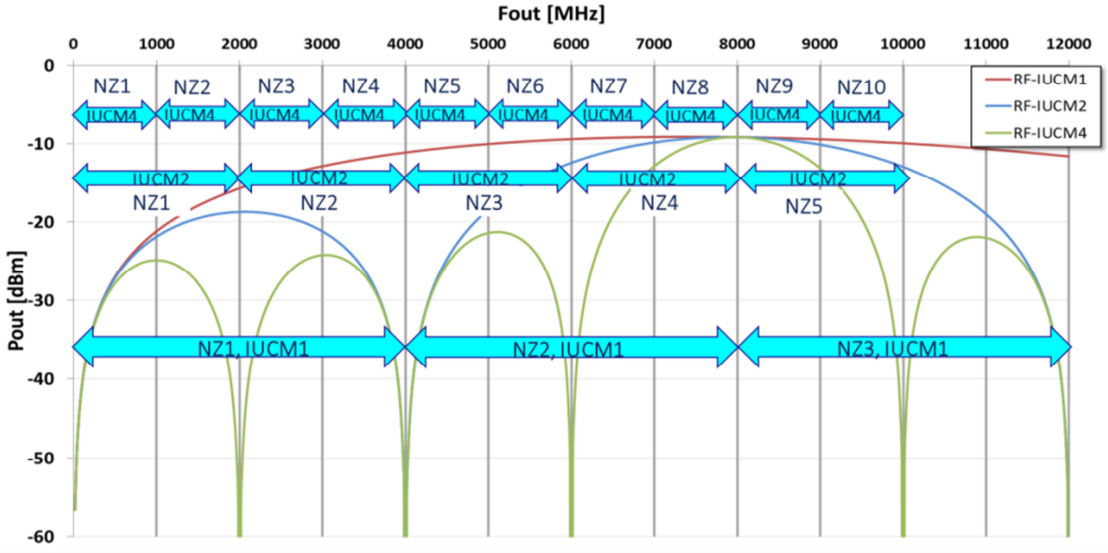
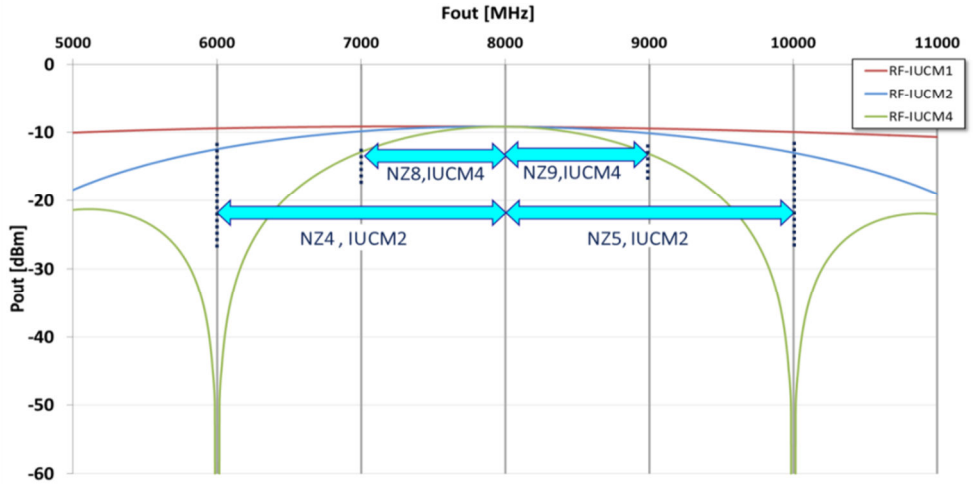


Figure 27. Pout curves at 8.0 GSps from DC to 12 GHz in IUCM1,IUCM2 and IUCM4 modes (Zoom around 8GHz)



Detailed explanation is given here-after for IUCM2 mode. IUCM4 mode is operating on the same principle but with a 4 division ratio.

In IUCM1 and 4:1 MUX modes, the input data rate is Fs/4 and the DSP clock is Fs/(2N*X), with N = MUX ratio (2 or 4) and X = OCDS ratio (1 or 2).

When the IUCM2 mode is selected, the input data rate becomes Fs/8 and the DSP clock frequency is Fs/(2N*X*2), with N = MUX ratio (2 or 4) and X = OCDS ratio (1 or 2). This means that in input under clocking mode, the DAC is capable to treat data at half the nominal rate. In this case, the DSP clock is also half its nominal speed. However, the sampling frequency stays the same.

Label	Logic Value	Description	Default setting
IUCM<1:0>	00 or 01	IUCM1: Input Under Clocking Mode inactive	00 (IUCM1)
	10	IUCM2: clock division ratio between DAC core and MUX: 2	
	11	IUCM4: clock division ratio between DAC core and MUX: 4	

The IUCM2 mode affects spectral response of the different modes.

The first effect is that Nyquist zone edges are no longer at n*Fclock/2 but at n*/Fclock/4 (this is the direct consequence of the division by 2 of the data rate).

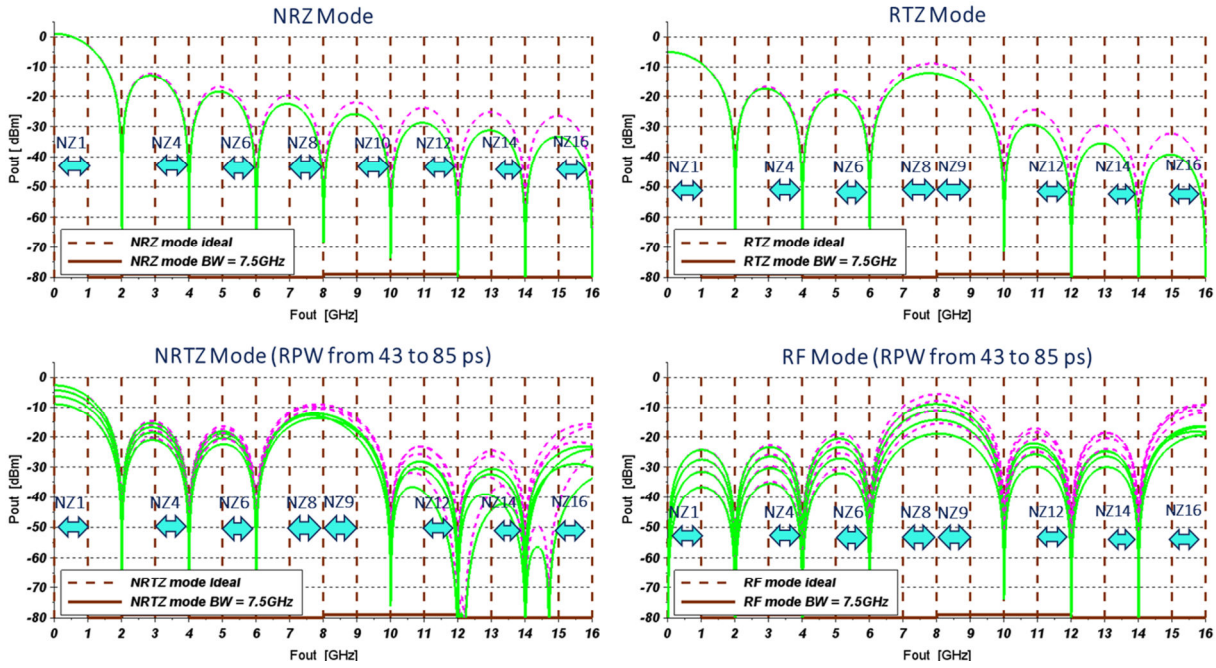
The second effect is the modification of the equations ruling the spectral responses in the different modes. For the 4 modes, the output power equations can be written (see section Mode Function 5.2 for IUCM1 ouput power):

$$\text{Pout\_IUCM2}(X) = \text{Pout\_IUCM1}.\cos(\pi.X)$$

$$\text{Pout\_IUCM4}(X) = \text{Pout\_IUCM1}.\cos(\pi.X).\cos(2\pi.X)$$

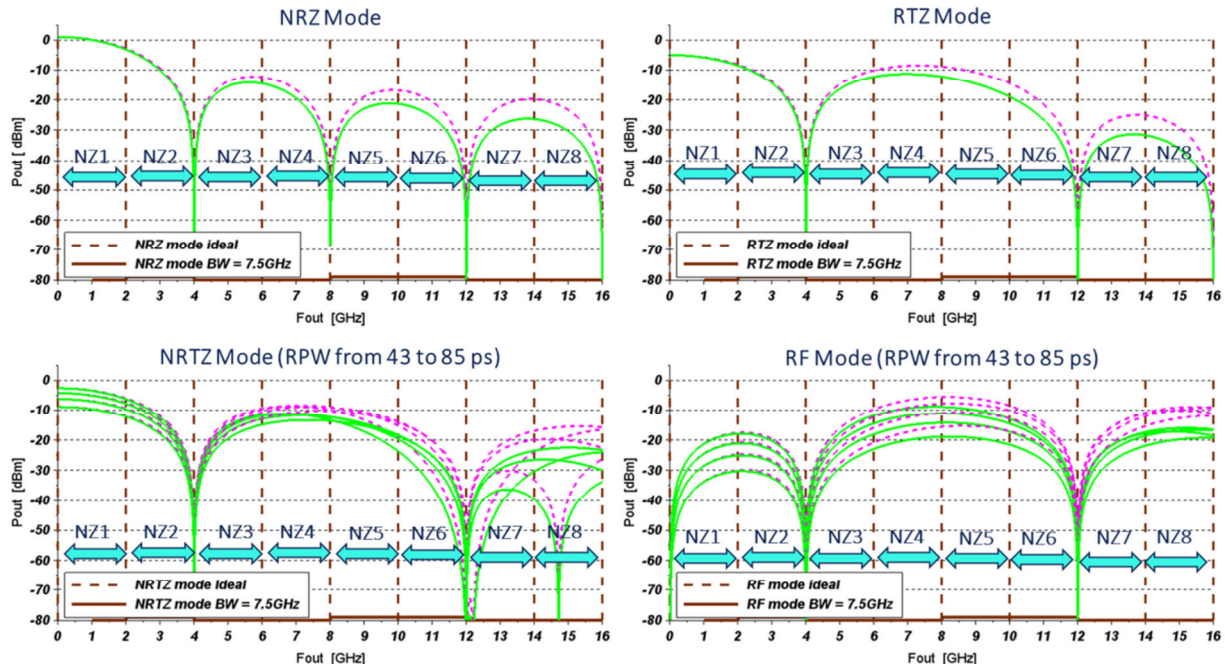
with X = Fout/Fclock

Figure 28 Max available Pout at nominal gain vs Fout in the four output modes at 8.0 GSps, combined with IUCM4, over 16 Nyquist zones, computed for different RPW steps



In RTZ, NRTZ and RF mode, the Output power is maximized in NZ8 and NZ9 (8th and 9th Nyquist zones)
At 8GSps with IUCM4, the Nyquist zones width is 1GHz.

Figure 29. Max available Pout at nominal gain vs Fout in the four output modes at 8.0 GSps, combined with IUCM2, over 16 Nyquist zones, computed for different RPW steps



In RTZ, NRTZ and RF mode, the Output power is maximized in NZ4 and NZ5 (4th and 5th Nyquist zones).
At 8GSps with IUCM2, the Nyquist zones width is 2GHz.

5.7 Multiplexer Delay Adjust (MDA)

MDA (Multiplexer Delay Adjust) is a setting allowing a fine-tuning of the sampling time, at the last Master/Slave clock stage of the MUX. MDA range varies from MDA0 to MDA5 (by steps of 14ps).
While it is not necessary to change its value default value (MDA2) when operating at 6.4 GSps/IUCM1, it is recommended to set it at MDA4 for 8.0 or 8.5 GSps (IUCM2 or IUCM4) operation, to optimize the performances.

5.8 Synchronization FPGA-DAC: IDC_P, IDC_N and TVF function

- IDC_P, IDC_N: Input Data Check function (LVDS signal).
- TVF: Timing Violation Flag.

The IDC_P, IDC_N signal are LVDS signals. This signal should be toggling at each cycle synchronously with other data bits.

This signal should be generated by the FPGA so that the DAC can check in real-time if the timings between the FPGA and the DAC are correct. The information on the synchronization is then given by the TVF flag.

IDC should be routed as the data signals (same layout rules and same length). It should be driven to an LVDS low or high level if not used.

Figure 30. IDC timing vs data input

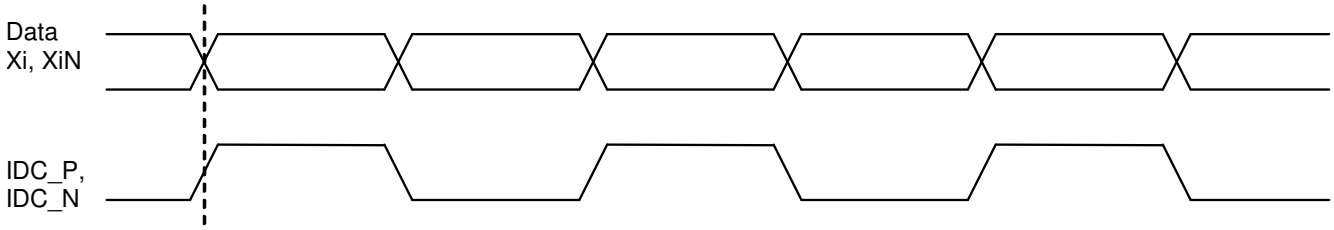
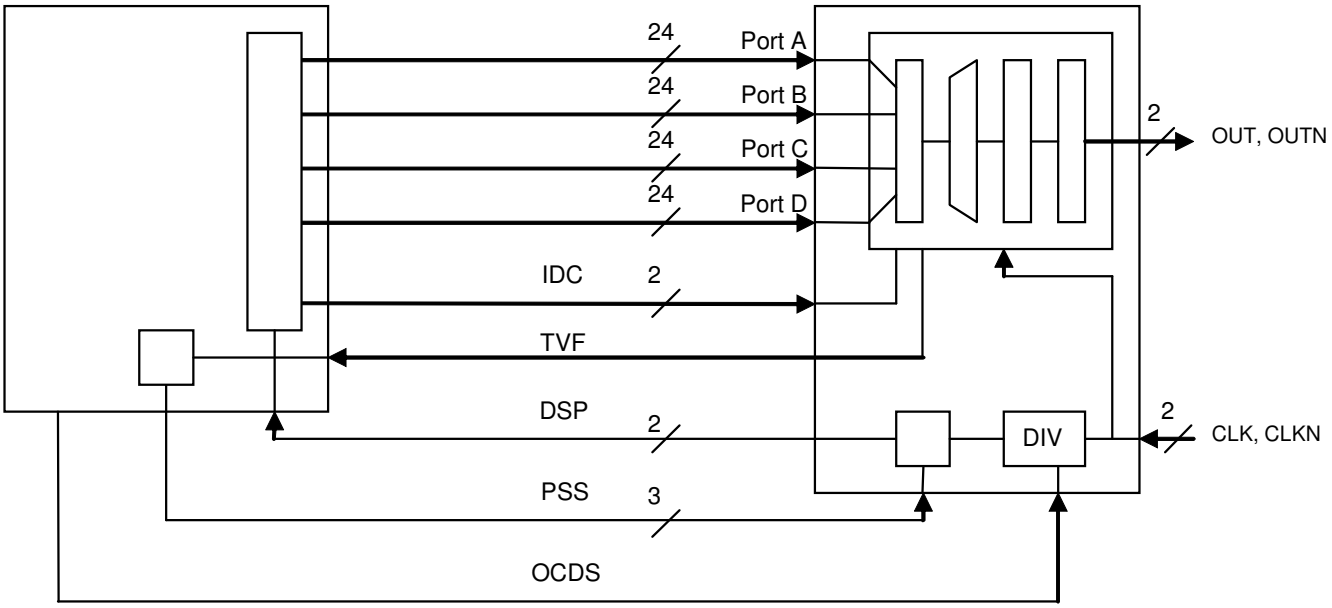


Figure 31. FPGA to DAC synoptic



TVF is a 3.3V output signal that indicates if the DAC and the FPGA are synchronised.

Table 17. TVF coding table

Label	Value	Description
TVF	0	SYNCHRO OK
	1	Data setup or hold time violation detected

Principle of Operation:

The IDC signal is sampled in parallel by 2 clocks. One is delayed positively by half a clock period, the other one is delayed negatively by half a clock period. The result of the sampling of the IDC input by both these clocks is then compared.

If both sampled outputs are equivalent, then TVF is at 0 to indicate that DAC and FPGA are synchronised. If not, TVF is set to 1 which means that the edge of the internal sampling clock is inside this window.

In that case it is recommended to either:

- Shift the DSP clock timing (possible by using the PSS function inside the DAC).
- Shift the phase of the FPGA PLL (if this functionality is available in the FPGA) to change the timing of the digital data compared to the DAC clock.

5.9 DSP output clock

The DSP output clock DSP, DSPN is an LVDS signal which is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock.

The DSP clock frequency is a fraction of the sampling clock frequency. The division factor depends on OCDS and IUCM settings. The DSP clock frequency is equal to (sampling frequency / [2N*X*M]) where N is the MUX ratio (2 or 4) and X is the output clock division factor (1 or 2), determined by the OCDS bit and M is the IUCM division ratio (1, 2 or 4) determined by the IUCM[1..0] value.

For example, in a 4:1 MUX ratio application with a sampling clock at 4 GHz and OCDS set to 0 (i.e. Factor of 1) and in IUCM1, then the input data rate is 1000 MSps and the DSP clock frequency is 500 MHz.

This DSP clock is used in the FPGA to control the digital data sequencing. Its phase can be adjusted thanks to the PSS[2:0] bits in order to ensure a proper synchronization between the data coming to the DAC and the sampling clock.

The TVF bit should be used to check whether the timing between the FPGA and the DAC is correct. When the IDC input is provided, the TVF will indicate if there are setup or hold violation at the DAC inputs. If any violation is detected through TVF, the PSS setting should be increased by 4 in MUX4 and by 2 in MUX2.

5.10 OCDS, IUCM and MUX combinations summary

The table here after gives the DSP clock division ratio with respect to the DAC input clock.

DSPclk = F_{CLK}/(2*N*M*X) DataRate = F_{CLK}/(N*M)

Where N: MUX Ratio (2 or 4), M: IUCM Ratio (1, 2 or 4), X: OCDS Ratio (1 or 2)

Table 18. OCDS, MUX, IUCM and PSS combinations summary

MUX Ratio		IUCM Ratio		OCDS Ratio		PSS Range / Steps	Input Data Rate
4:1	0	IUCM1	00	OCDS1: DSP Clock = F_{CLK}/8	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/4
				OCDS2: DSP Clock = F_{CLK}/16	1		
		IUCM2	10	OCDS1: DSP Clock = F_{CLK}/16	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/8
				OCDS2: DSP Clock = F_{CLK}/32	1		
		IUCM4	11	OCDS1: DSP Clock = F_{CLK}/32	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/16
				OCDS2: DSP Clock = F_{CLK}/64	1		
2:1	1	IUCM1	00	OCDS1: DSP Clock = F_{CLK}/4	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/2
				OCDS2: DSP Clock = F_{CLK}/8	1		
		IUCM2	10	OCDS1: DSP Clock = F_{CLK}/8	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/4
				OCDS2: DSP Clock = F_{CLK}/16	1		
		IUCM4	11	OCDS1: DSP Clock = F_{CLK}/16	0	0 to 7/(2*F_{CLK}) 1/(2*F_{CLK}) steps	F_{CLK}/8
				OCDS2: DSP Clock = F_{CLK}/32	1		

Notes:

1. Behaviour according to MUX, OCDS, IUCM and PSS combination is independent of output mode.
2. In 2:1 MUX, only 4 steps of PSS are useful, the 4 other gives the same result.

5.11 Synchronization function

The timer of the DAC must be reset after the following changes of configuration:

- At power-on;
- Whenever one of the following parameter is modified: OCDS, MUX or IUCM;
- Whenever the master clock is modified (amplitude, frequency...).

There are two SYNC functions integrated in this DAC which reset its timer:

- A power up reset, which is triggered by the power supplies if the dedicated power up sequence is applied V_{CCD} -> V_{CCA3} ->V_{CCA5} (the clock must be supplied to the DAC prior to this power up sequence being generated);
- An external SYNC, which is triggered by a pulse applied to the differential SYNC/SYNCN inputs.
- At power-on, there are 2 possibilities:
- The power-up sequence of the DAC is V_{CCD}, V_{CCA3} then V_{CCA5}. In that case an internal power on reset is generated by the DAC. There is no need to send a SYNC pulse as long as OCDS, MUX or IUCM and the master clock are not modified (see Section 7.8 for more information).
- If the power-up sequence is different from the one above, a SYNC pulse must be sent to the DAC.

The external SYNC is LVDS compatible. It is active high. After the application of the SYNC signal, the DSP clock from the DAC will stop and after a constant and known time (t_{DSP}); the DSP clock will start up again.

The external SYNC can also be used to synchronize multiple DACs.

The pulse duration should be at least of 3 master clock cycles in OCDS1 and IUCM1.

Depending on the settings of OCDS, IUCM and also on the MUX ratio the width of the SYNC pulse must be greater than a certain number of external clock pulses. It is also necessary that the sync pulse width shall be a whole number of clock cycles.

5.12 Gain Adjust function

This function allows the adjustment of the internal gain of the DAC so that it can be tuned to the unity gain.

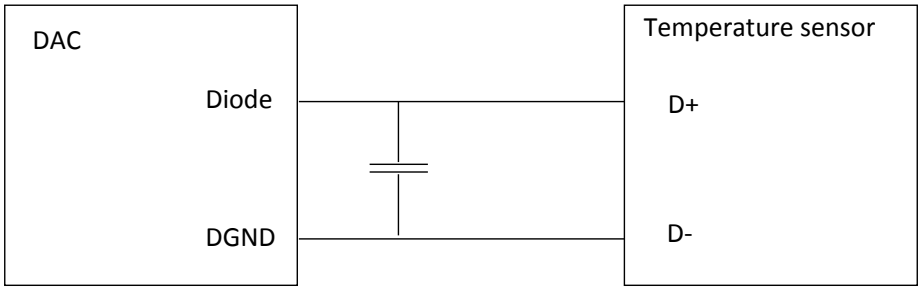
The gain of the DAC can be adjusted by setting the GAIN register through the 3WSI. The gain can be adjusted by 1024 steps. GA min is given for GAIN = 0x000 and GA max for GAIN = 0x3FF. Default value is GA typ given for GAIN = 0x200.

Note: The gain voltage step is indicated in Section 3.3 Table 3. DC Electrical characteristics

5.13 Diode function

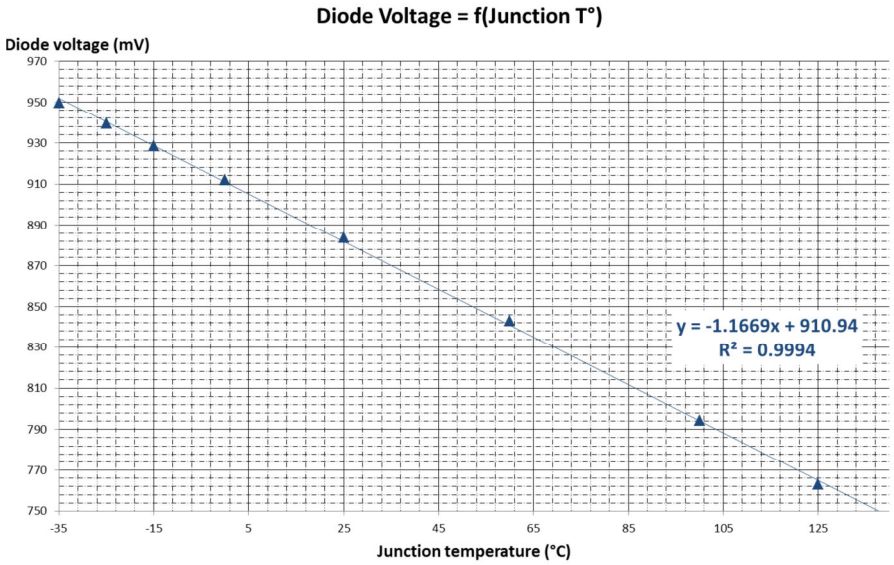
A diode for die junction temperature monitoring, is available in this DAC. For the measurement of die junction temperature, a temperature sensor can be used.

Figure 32. Temperature diode implementation



In characterization measurement a current of 1 mA is applied on the DIODE pin. The voltage across the DIODE pin and the DGND pin gives the junction temperature using the intrinsic diode characteristics below.

Figure 33. Diode Characteristics for Die Junction Temperature Monitoring



5.14 DAC 3WSI Description (DAC Controls)

5.14.1 3WSI timing description

The 3WSI is a synchronous write only serial interface made of 4 signals:

reset_n : asynchronous 3WSI reset, active low sclk : serial clock input

sld_n : serial load enable input sdata : serial data input.

The 3WSI gives a write-only access to up to 16 different internal registers of up to 12 bits each. The input format is fixed with 4 bits of register address followed by 12 bits of data. Address and data are sent MSB first.

The write procedure is fully synchronous with the clock rising edge of sclk and described in the following chronogram.

sld_n and sdata are sampled on each rising clock edge of sclk (clock cycle). sld_n must be set at 1 when no write procedure is done.

A write starts on the first clock cycle when sld_n is at 0. sld_n must stay at 0 during the complete write procedure.

In the first 4 clock cycles with sld_n at 0, 4 bits of register address from MSB (a[3]) to LSB (a[0]) are entered.

In the next 12 clock cycles with sld_n at 0, 12 bits of data from MSB (d[11]) to LSB (d[0]) are entered. This gives 16 clock cycles with sld_n at 0 for a normal write procedure.

A minimum of one clock cycle with sld_n returned at 1 is requested to end the write procedure, before the interface is ready for a new write procedure. Any clock cycle with sld_n at 1 before the write procedure is completed interrupts this procedure and no data transfer to internal registers is done. It is possible to have only one clock cycle with sld_n at 1 between two following write procedures.

Additional clock cycles with sld_n at 0 after the parallel data have been transferred to the register do not affect the write procedure and are ignored.

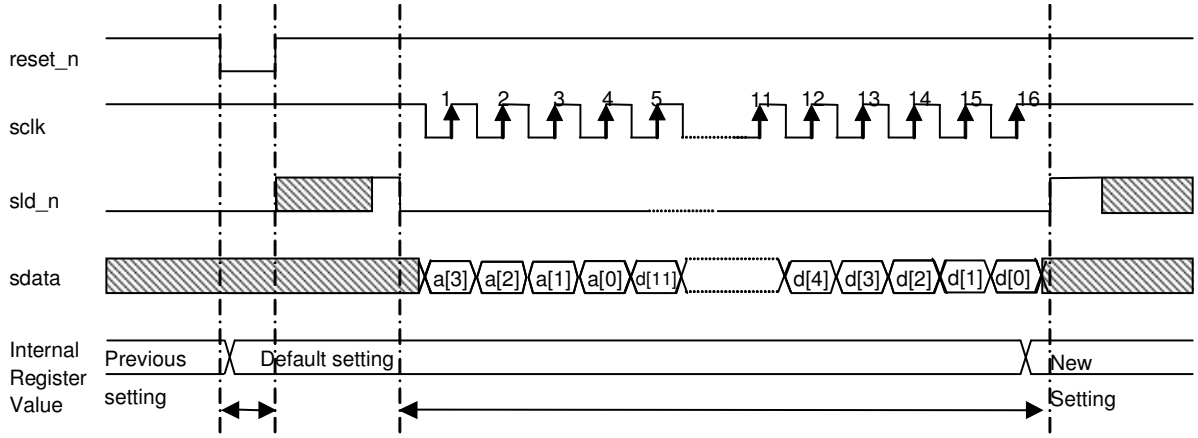
12 bits of data must always be sent, even if the internal addressed register has less than 12 bits. Unused bits (usually MSB's) are ignored. Bit signification and bit position for the internal registers are detailed in the section Registers .

The reset_n pin combined with the sld_n pin can be used as a reset to program the chip to the reset setting.

reset_n high: no effect

reset_n low and sld_n low: programming of registers to default values

Figure 34. 3WSI Timing Diagram



Timings related to 3WSI are given in the table below

Table 19. 3WSI Timings

Name	Parameter	Min	Typ	Max	Unit	Note
Tsclk	Period of sclk	1			µs	
Twsclk	High or low time of sclk	0.5			µs	
Tssld_n	Setup time of sld_n before rising edge of sclk	4			µs	
Thsld_n	Hold time of sld_n after rising edge of sclk	2			µs	
Tssdata	Setup time of sdata before rising edge of sclk	4			ns	
Thsdata	Hold time of sdata after rising edge of sclk	2			ns	
Twlreset	Minimum low pulse width of reset_n	5			ns	
Tdreset	Minimum delay between an edge of reset_n and the rising edge of sclk	5			µs	

5.14.2 3WSI: Address and Data Description

This 3WSI is activated with the control bit sld_n going low (please refer to write timing in next section). The length of the word is 16 bits: 12 for the data and 4 for the address.

The maximum serial logic clock frequency is 1 MHz.

Table 20. Registers Mapping

Address	Label	Description	Default Setting
0000	State Register	MUX ratio Selection Output MODE selection IUCM ratio selection External Control for DSP Clock Reshaping Pulse Width (RPW) adjust Reshaping Pulse Begin (RPB) adjust	0x922
0001	GA Register	Gain Adjust register	0x200
0010		Not available	
0011		Not available	
0100		Not available	
0101	DSP Register	MDA, PSS, OCDS controls	0x080
0110		Not available	
0111		Not available	
1000 to 1111		Not available	

5.14.3 State Register (address 0000)

Table 21. State register Mapping (Address 0000)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RPW<2:0>			RPB<2:0>			ECDC	IUCM<1:0>		MODE<1:0>		MUX

Default value: 0x922

Table 22. State register Coding (Address 0000)

Label		Coding	Description	Default Value	Notes
MUX	D0	0	4:1 MUX mode	0	(1)
		1	2:1 MUX mode		
MODE<1:0>	D2,D1	00	NRZ mode	01	(1)
		01	Narrow RTZ (a.k.a. NRTZ) mode		
		10	RTZ Mode		
		11	RF mode		
IUCM<1:0>	D4, D3	00	IUCM1 (MUX at DAC core speed)	00	(1)
		01	IUCM1 (MUX at DAC core speed)		
		10	IUCM2 (MUX at DAC core speed/2)		
		11	IUCM4 (MUX at DAC core speed/4)		
ECDC	D5	0	OCDS and PSS ruled by DSP register at address 0101	1	(1)(2)
		1	OCDS and PSS externally controlled		
RPB<2:0>	D8, D7, D6	000	RPB2 = 38 ps	100	(3)
		001	RPB2 = 38 ps		
		010	RPB0 = 12ps		
		011	RPB1 = 25 ps		
		100	RPB2 = 38 ps		
		101	RPB3 = 51 ps		
		110	RPB4 = 64 ps		
		111	RPB2 = 38 ps		
RPW<2:0>	D11, D10, D9	000	RPW2 66 ps in NRTZ mode / 68 ps in RF mode	100	(4)
		001	RPW2 66 ps in NRTZ mode / 68 ps in RF mode		
		010	RPW0 43 ps in NRTZ mode / 52 ps in RF mode		
		011	RPW1 49 ps in NRTZ mode / 60 ps in RF mode		
		100	RPW2 66 ps in NRTZ mode / 68 ps in RF mode		
		101	RPW3 78 ps in NRTZ mode / 86 ps in RF mode		(5)
		110	RPW4 56 ps in NRTZ mode / 76 ps in RF mode		
		111	RPW2 66 ps in NRTZ mode / 68 ps in RF mode		

Notes:

1. Default mode is 4:1 MUX, NRTZ output mode, IUCM1, and PSS & OCDS externally controlled. Default mode is programmed by power up reset or low level pulse on *reset_n* pin while *sld_n* pin is low.
2. ECDC: when ECDC is High the timing of the DSP clock is controlled externally through pins PSS<2:0> and OCDS; when ECDC is low, this functionality is controlled through the 3WSI by the DSP register at address 0101.
3. RPB setting is applicable in NRTZ, RTZ and RF modes. RPB values are design values.
4. RPW setting is applicable in NRTZ and RF modes. RPW values are typical values measured on one part.
5. From design, in case RPW> Tclk/2, the RPW value becomes equal to Tclk – RPW. For example at Fclk = 6.4 GHz, it affects the largest RPW value (RPW4=100ps) which will then become 156 – 100 = 56 ps. This largest RPW value will be affected for Fclk above 5 GHz (for which RPW4=100ps becomes superior to Tclk/2).

5.14.4 GA Register (address 0001)

Table 23. GA register Mapping (Address 0001)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		GA<9:0>									

Default value: 0x200

5.14.5 DSP Register (address 0101)

Table 24. DSP register Mapping (Address 0101)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				MDA<2:0>			PSS<2:0>				OCDS

Default value: 0x080 (OCDS = 0, PSS = 000)

Table 25. Registers 0000 to 0101 Summary

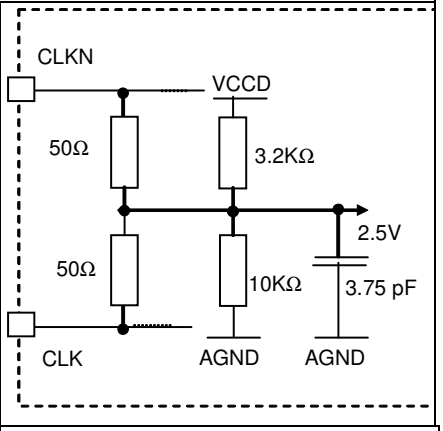
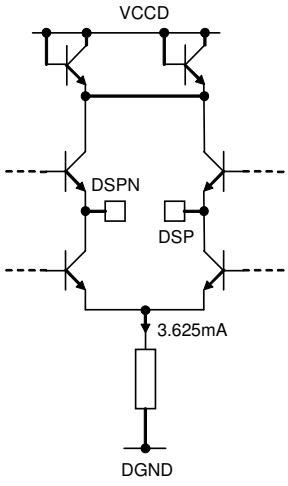
Address	Description	Default register value	Default parameter value	Register value for max value	Parameter max value	Register value for min value	Parameter min value	Step
0000	RPB Adjust	0x922	RPB2	0x9A2	RPB4	0x8A2	RPB0	1 bit
0000	RPW Adjust	0x922	RPW2	0xD22	RPW4	0x522	RPW0	1 bit
0000	ECDC	0x922	ECDC1	0x922	ECDC1	0x902	ECDC0	N/A
0000	IUCM	0x922	IUCM1	0x93A	IUCM4	0x922	IUCM1	N/A
0000	MODE	0x922	NRTZ	0x926	RF	0x920	NRZ	N/A
0000	MUX	0x922	4:1 MUX	0x923	2:1 MUX	0x922	4:1 MUX	N/A
0001	Gain Adjust	0x200	1	0x3FF	1.15	0x000	0.85	300ppm
0101	PSS	0x080	PSS0	0x09C	PSS7	0x080	PSS0	N/A
0101	OCDS	0x080	OCDS1	0x081	OCDS2	0x080	OCDS1	N/A
0101	MDA	0x080	MDA2	0x0E0	MDA5	0x080	MDA0	N/A

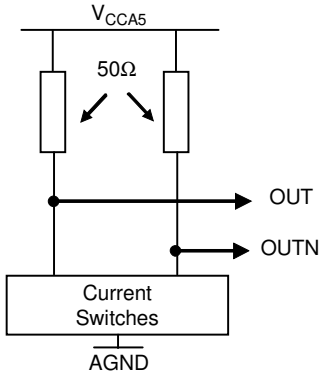
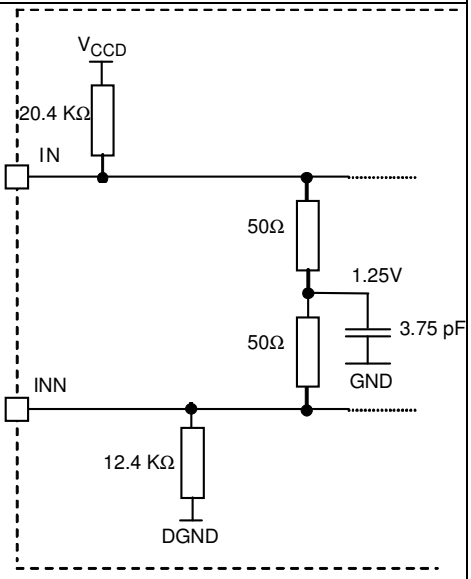
6. PIN DESCRIPTION

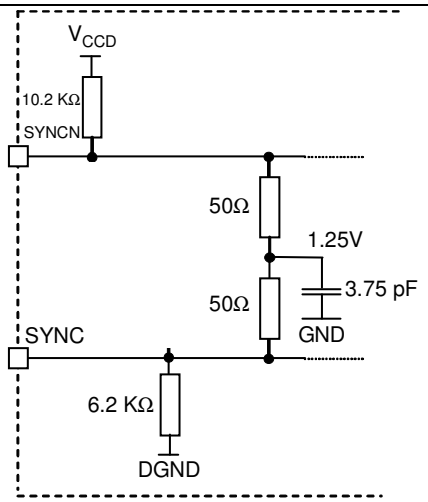
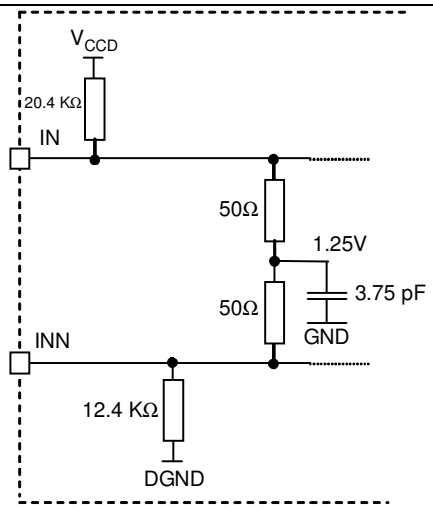
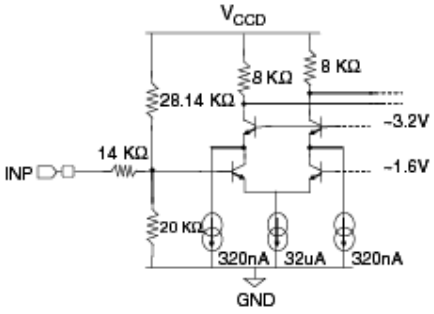
Figure 35. Pinout view fpBGA196 (Top view)

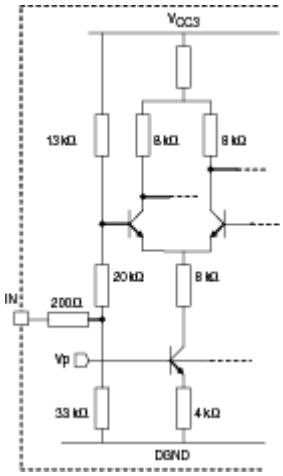
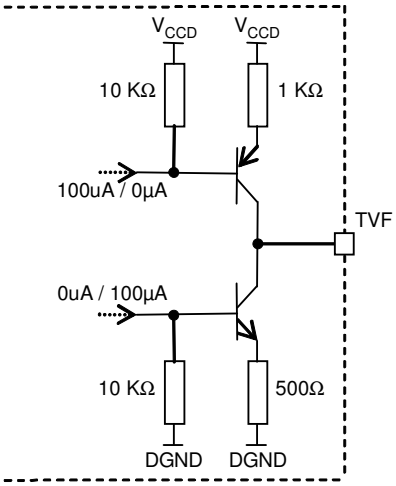
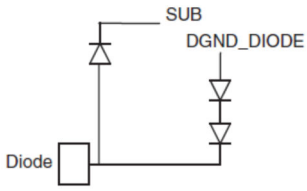
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	B5	B6	B6N	B9	B9N	B11	C11	C9N	C9	C6N	C6	C5	DGND	A
B	B3	B4	B5N	B7	B8	B10	B11N	C11N	C10	C8	C7	C5N	C4	C3	B
C	B1N	B3N	B4N	B7N	B8N	B10N	DGND	DGND	C10N	C8N	C7N	C4N	C3N	C1N	C
D	B1	B2	B2N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C2N	C2	C1	D
E	A10N	B0	B0N	DGND	DGND	VCCD	VCCD	VCCD	VCCD	DGND	DGND	C0N	C0	D10N	E
F	A10	A11	A11N	VCCD	VCCD	AGND	AGND	AGND	AGND	VCCD	VCCD	D11N	D11	D10	F
G	A8	A8N	A9	A9N	DGND	AGND	AGND	AGND	AGND	DGND	D9N	D9	D8N	D8	G
H	A6	A6N	A7	A7N	DGND	AGND	AGND	AGND	AGND	DGND	D7N	D7	D6N	D6	H
J	A3N	A5	A5N	VCCA3	VCCA3	AGND	AGND	AGND	AGND	VCCA3	VCCA3	D5N	D5	D3N	J
K	A3	A4	A4N	DGND	DGND	AGND	VCCA5	VCCA5	AGND	DGND	DGND	D4N	D4	D3	K
L	A1N	A2	A2N	DGND	Diode	VCCA5	VCCA5	VCCA5	VCCA5	DGND	sldn	D2N	D2	D1N	L
M	A1	A0N	NC	TVF	reset_n	VCCA5	VCCA5	AGND	AGND	sdata	sclk	PSS2	D0N	D1	M
N	A0	DSPN	IDC_P	SYNCN	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	iref_test	OCDS	D0	N
P	DGND	DSP	IDC_N	SYNC	CLK	AGND	AGND	AGND	OUT	OUTN	AGND	PSS0	PSS1	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 26. Pinout Table fpBGA196

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Power supplies				
V_{CCA5}	K7, K8, L6, L7, L8, L9, M6, M7	5.0V analog power supplies Referenced to AGND	N/A	
V_{CCA3}	J4, J5, J10, J11	3.3V analog power supply Referenced to AGND	N/A	
V_{CCD}	D6, D7, D8, D9, E6, E7, E8, E9, F4, F5, F10, F11	3.3V digital power supply Referenced to DGND	N/A	
AGND	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K6, K9, M8, M9, N6, N7, N8, N9, N10, N11, P6, P7, P8, P11	Analog Ground	N/A	
DGND	A1, A14, C7, C8, D4, D5, D10, D11, E4, E5, E10, E11, G5, G10, H5, H10, K4, K5, K10, K11, L4, L10, P1, P14	Digital Ground	N/A	
Clock signals				
CLK CLKN	P5 N5	Master sampling clock input (differential) with internal common mode at 2.5V It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	
DSP DSPN	P2 N2	Output clock (in-phase and inverted phase) If not used, should be 100Ω terminated.	O	

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
Analog output signal				
OUT OUTN	P9, P10	In phase and inverted phase analog output signal (differential termination required)	O	
Digital Input signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	N1, M2 M1, L1 L2, L3 K1, J1 K2, K3 J2, J3 H1, H2 H3, H4 G1, G2 G3, G4 F1, E1 F2, F3	Differential Digital input Port A Data A0, A0N is the LSB Data A11, A11N is the MSB		
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	E2, E3 D1, C1 D2, D3 B1, C2 B2, C3 A2, B3 A3, A4 B4, C4 B5, C5 A5, A6 B6, C6 A7, B7	Differential Digital input Port B Data B0, B0N is the LSB Data B11, B11N is the MSB		
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N C10, C10N C11, C11N	E13, E12 D14, C14 D13, D12 B14, C13 B13, C12 A13, B12 A12, A11 B11, C11 B10, C10 A10, A9 B9, C9 A8, B8	Differential Digital input Port C Data C0, C0N is the LSB Data C11, C11N is the MSB	I	

Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N D10, D10N D11, D11N	N14, M13 M14, L14 L13, L12 K14, J14 K13, K12 J13, J12 H14, H13 H12, H11 G14, G13 G12, G11 F14, E14 F13, F12	Differential Digital input Port D Data D0, D0N is the LSB Data D11, D11N is the MSB	I	
Control signals				
SYNC, SYNCN	P4, N4	In phase and Inverted phase reset signal	I	
IDC_P, IDC_N	N3, P3	Input data check	I	
sdata	M10	3WSI serial data input.	I	
sclk	M11	3WSI clock.		
reset_n	M5	Reset for the 3WSI registers		
sld_n	L11	3WSI serial load enable input.		
OCDS	N13	Output Clock Division Select	I	Driven by resistor: 10Ω or 10 KΩ

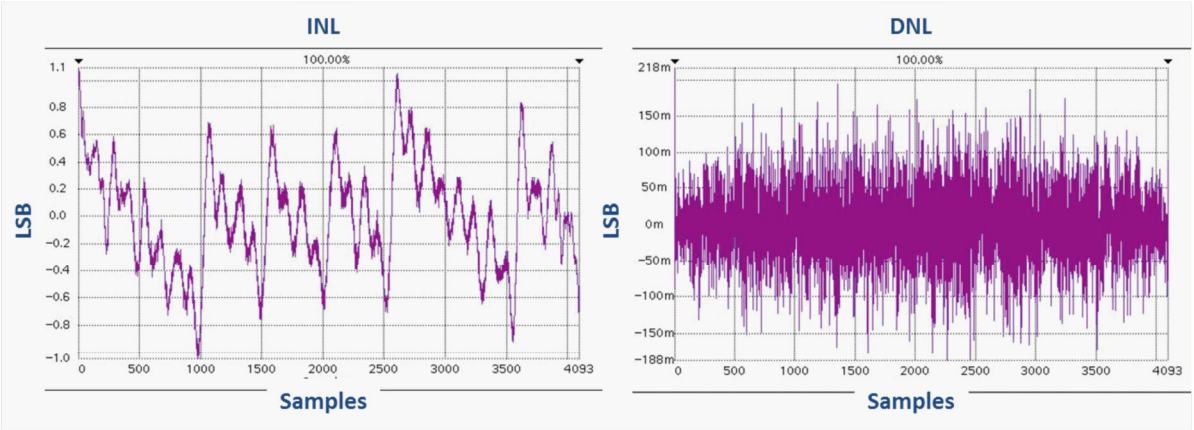
Signal name	Pin number	Description	Direction	Equivalent Simplified schematics
PSS0 PSS1 PSS2	P12 P13 M12	Phase Shift Select (PSS2 is the MSB)		Driven by voltage: < 0.5 V or > 2 V 
TVF	M4	Setup/Hold time violation flag	O	
Diode	L5	Diode for die junction temperature monitoring	I	
Iref test	N12	Bandgap output for test purpose. To leave unconnected	O	
NC	M3	Not connected		

6 CHARACTERIZATION RESULTS

6.1 Static performance

6.1.1 INL/DNL

Figure 36. INL & DNL measurements at Fout = 100 kHz, Fclock = 3 GHz



6.1.2 DC Gain

Figure 37. Output Voltage variations versus Gain Adjust

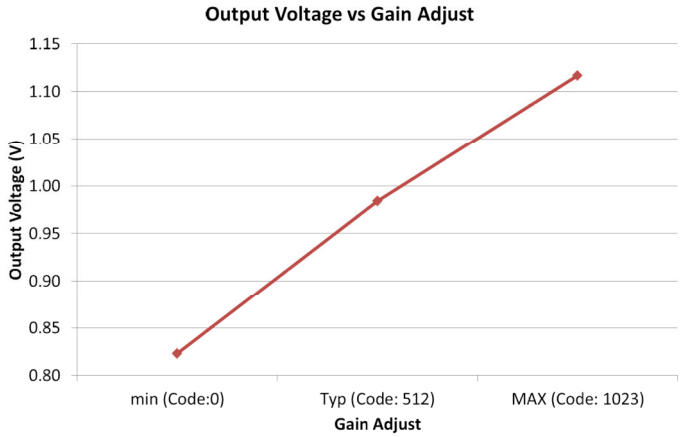
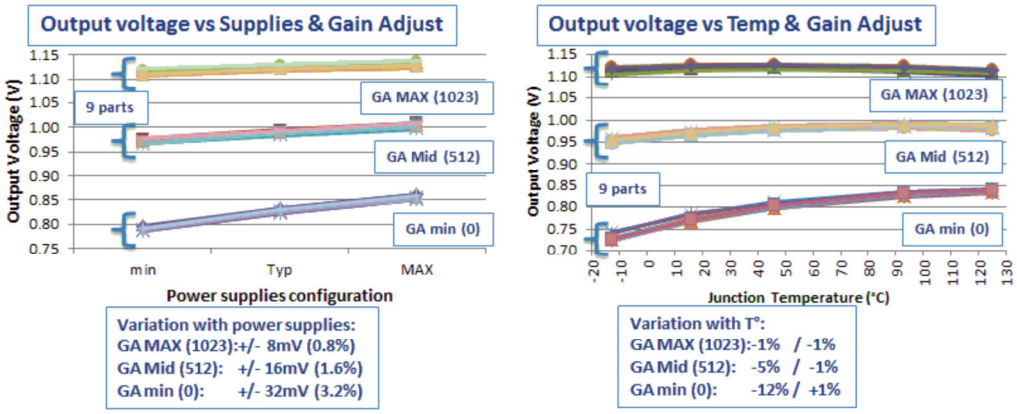


Figure 38. Output voltage variation vs Power supplies & temperature vs Gain Adjust



6.2 AC performance

6.2.1 Available Output Power vs Fout.

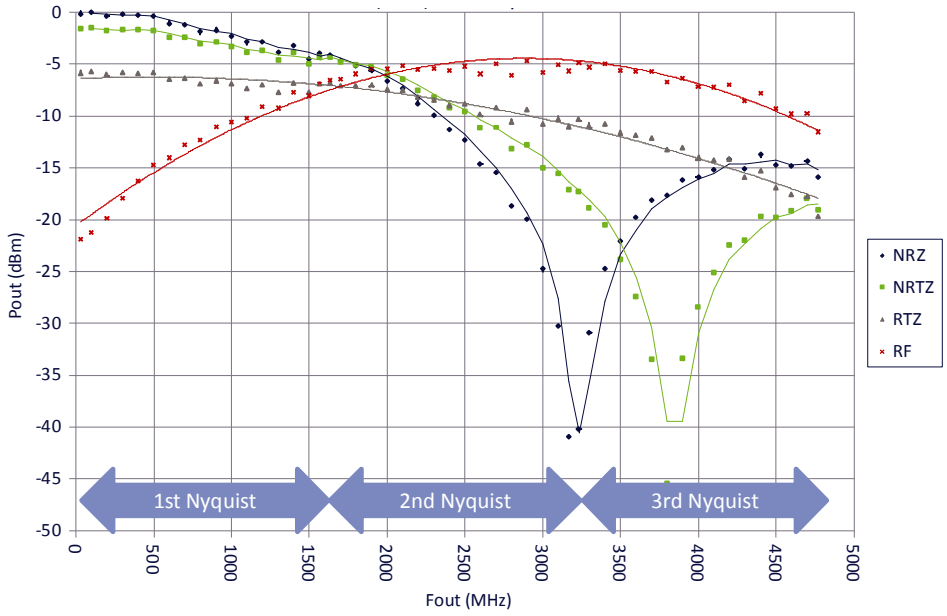
NRZ mode offers max power for 1st Nyquist operation.

NRTZ mode offers optimum power over full 1st and first half of 2nd Nyquist zones. RTZ mode offers slow roll off for 2nd Nyquist operation.

RF mode offers maximum power over 2nd and 3rd Nyquist operation. It is globally the most suitable mode for operation up to the 8th Nyquist.

6.2.1.1 MUX 2:1 at 3.2 GSps

Figure 39. Pout vs Fout from 32 MHz to 4768 MHz in the 4 output modes at 3.2 GSps in MUX2:1



6.2.1.2 MUX 4:1 at 6.4 GSps

Measurements from DC to 6.4 GHz are carried out with the Marki Bal10 [200 kHz - 10 GHz] balun (ref BAL-0010).
Measurements from 6.4 to 26 GHz are carried out with Krytar [6 GHz - 26.5 GHz] balun (ref 4060265).

Figure 40. Pout vs Fout @ 6.4 GSps from DC to 9 GHz vs modes

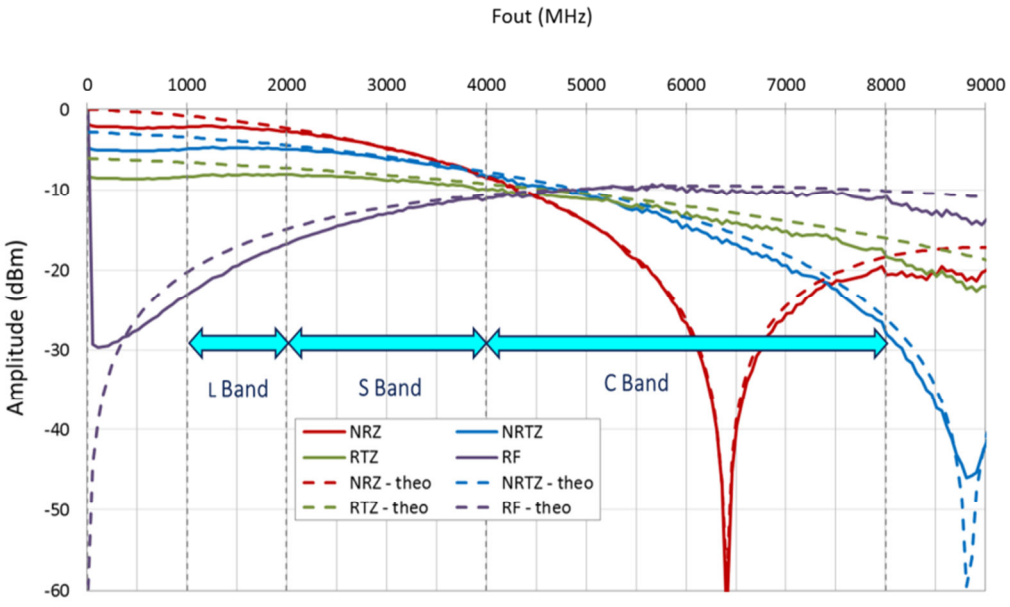


Figure 41. Pout vs Fout @ 6.4 GSps from 8 GHz to 26 GHz vs modes (includes X-Band, Ku-Band and K Band)

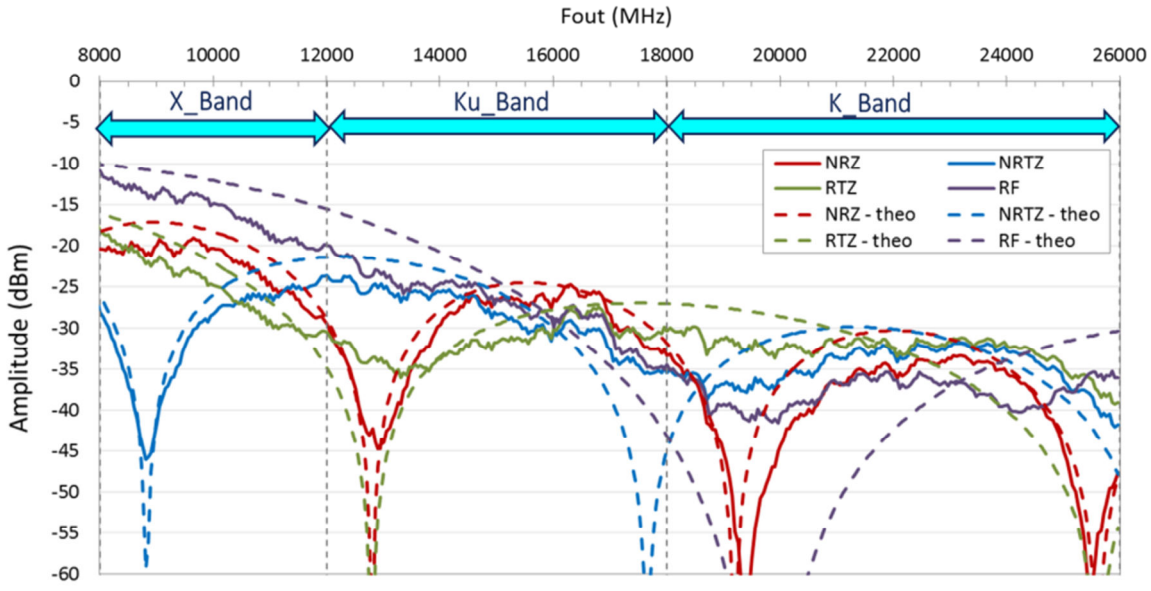


Figure 42. Pout vs Fout @ 6.4 GSps from 8 GHz to 12 GHz vs modes (X-Band)

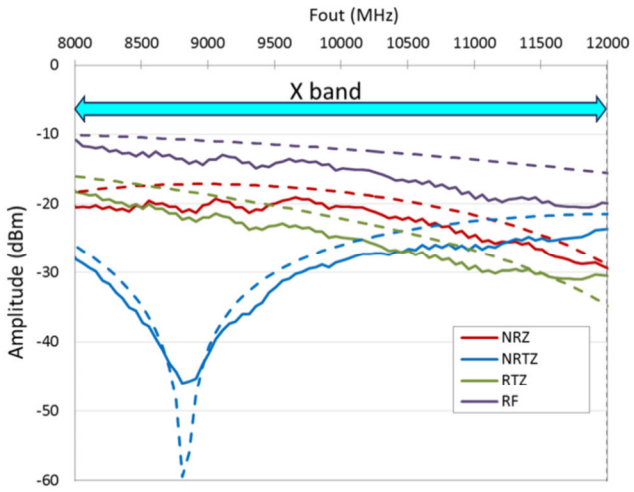


Figure 43. Pout vs Fout @ 6.4 GSps from 12 GHz to 18 GHz vs modes (Ku-Band)

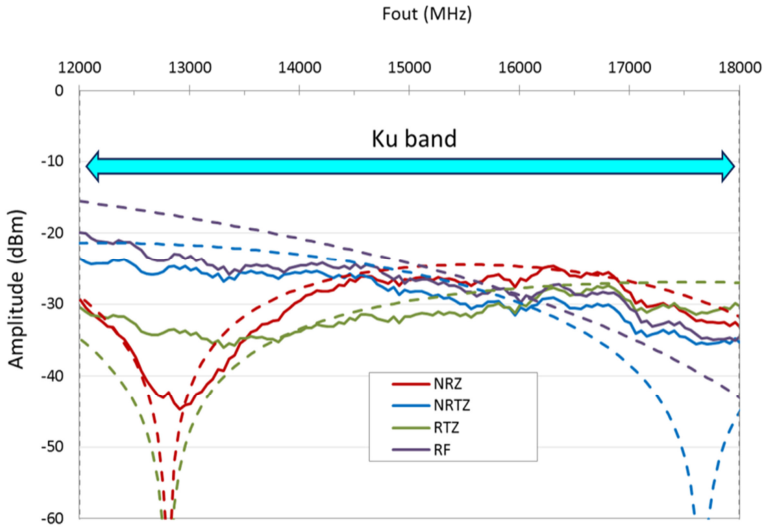
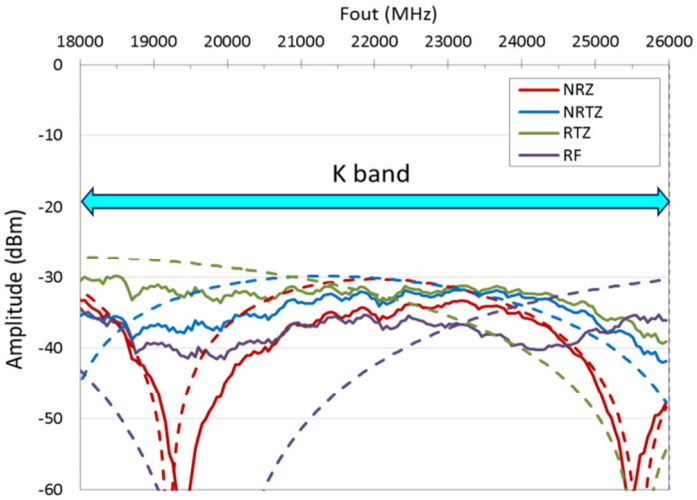


Figure 44. Pout vs Fout @ 6.4 GSps from 12 GHz to 26 GHz vs modes (K-Band)



6.2.1.3 MUX 4:1 at 8.0 GSps, modes IUCM2 and IUCM4

Note : IUCM1 at 8.0 and 8.5 Gsps curve is given for reference only and cannot be used due to FPGA output data rate limitation (The maximum sampling rate in IUCM1 is 7Gsps).

Figure 45. Pout vs Fout @ 8.0 GSps from DC to 26 GHz, IUCM1, IUCM2 and IUCM4 in RF mode

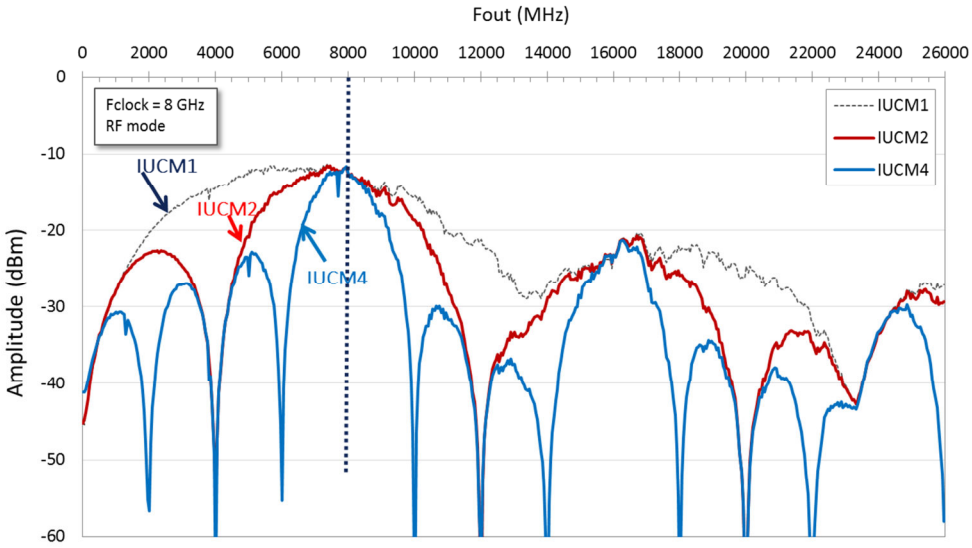


Figure 46. Pout vs Fout @ 8.0 GSps from 5GHz to 11 GHz , IUCM1, IUCM2 and IUCM4 in RF mode

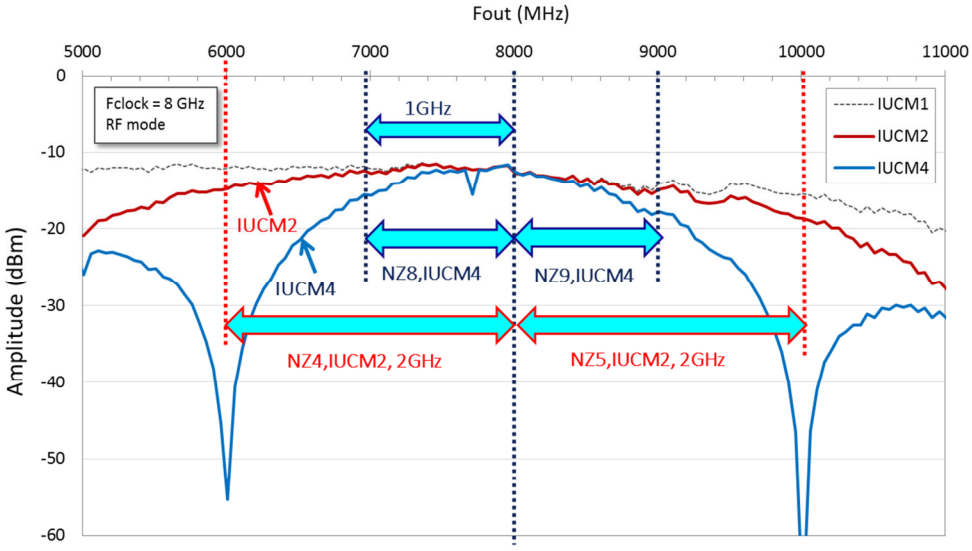


Figure 47. Pout vs Fout @ 8.5 GSps from DC to 26 GHz , IUCM1, IUCM2 and IUCM4 in RF mode

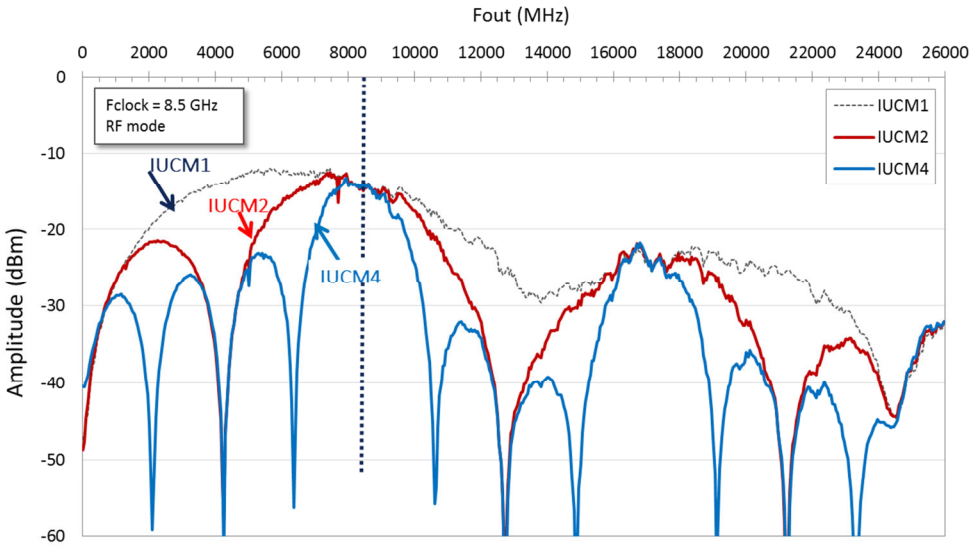
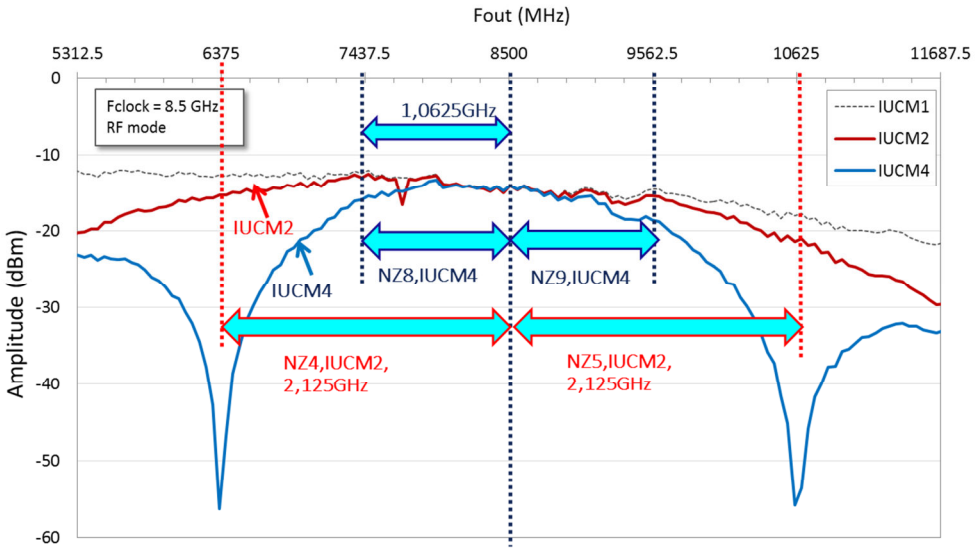


Figure 48. Pout vs Fout @ 8.5 GSps from 5.3125 GHz to 11.6875 GHz , IUCM1, IUCM2 and IUCM4 in RF mode



6.2.2 Single Tone SFDR Measurements versus Fout

Figure 7-15 summarizes SFDR measurements in MUX4:1 mode, for an Fout sweep from 50 MHz to 8999 MHz.

Figure 7-16 summarizes SFDR measurements in MUX2:1 mode, for an Fout sweep from 32 MHz to 4768 MHz.

Figure 7-17 summarizes SFDR measurements in MUX4:1 mode, for an Fout sweep from 5 GHz to 24 GHz in RF mode.

Figure 49. SFDR in the 4 output modes at 6.4 GSps in MUX4:1

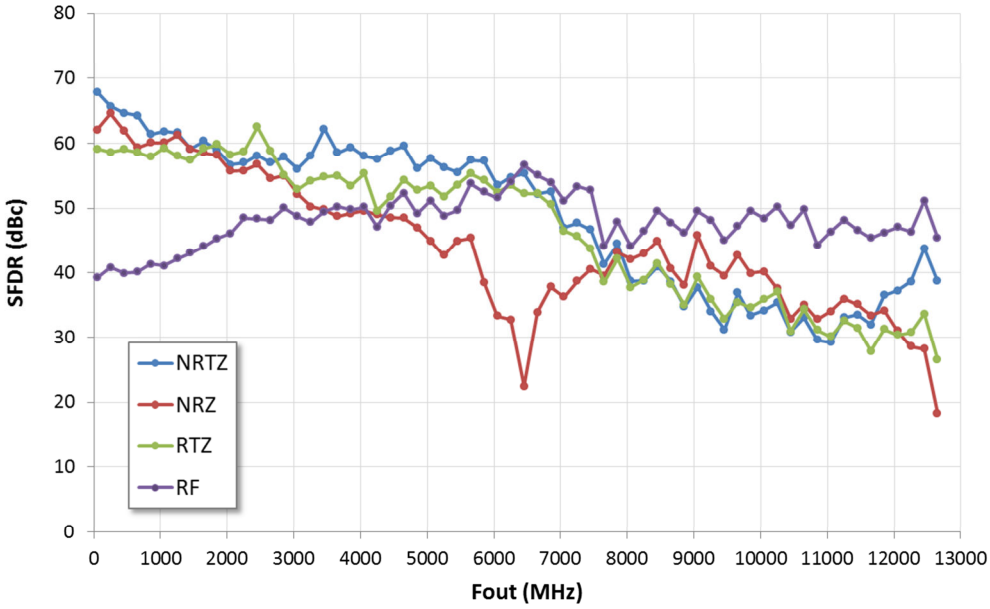


Figure 50. SFDR in the 4 output modes at 3.2 GSps in MUX2:1

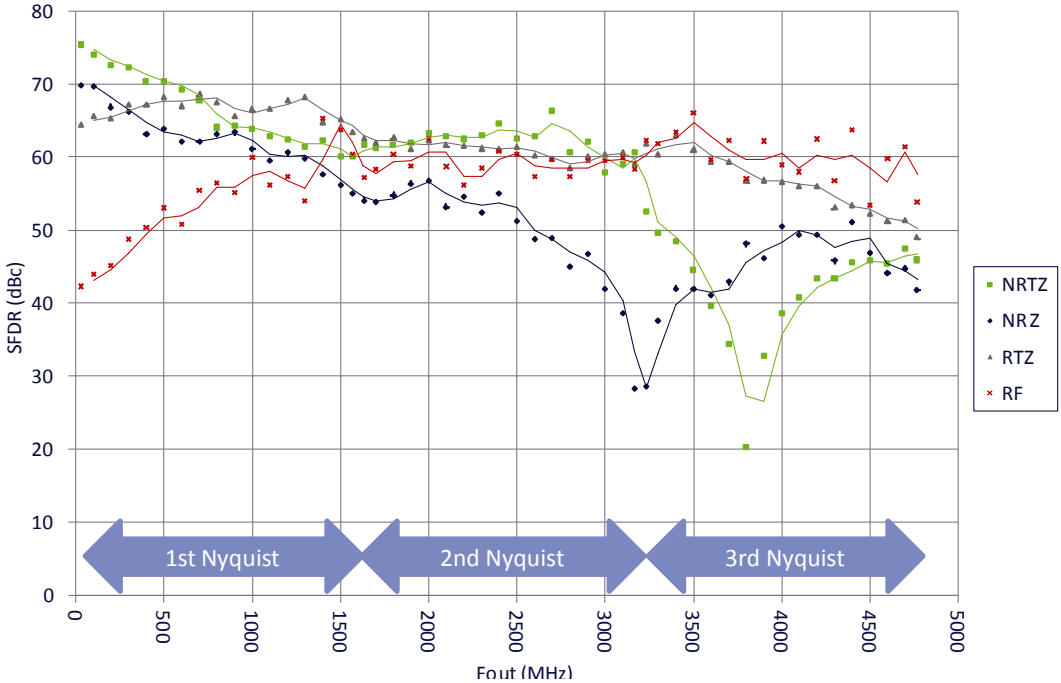
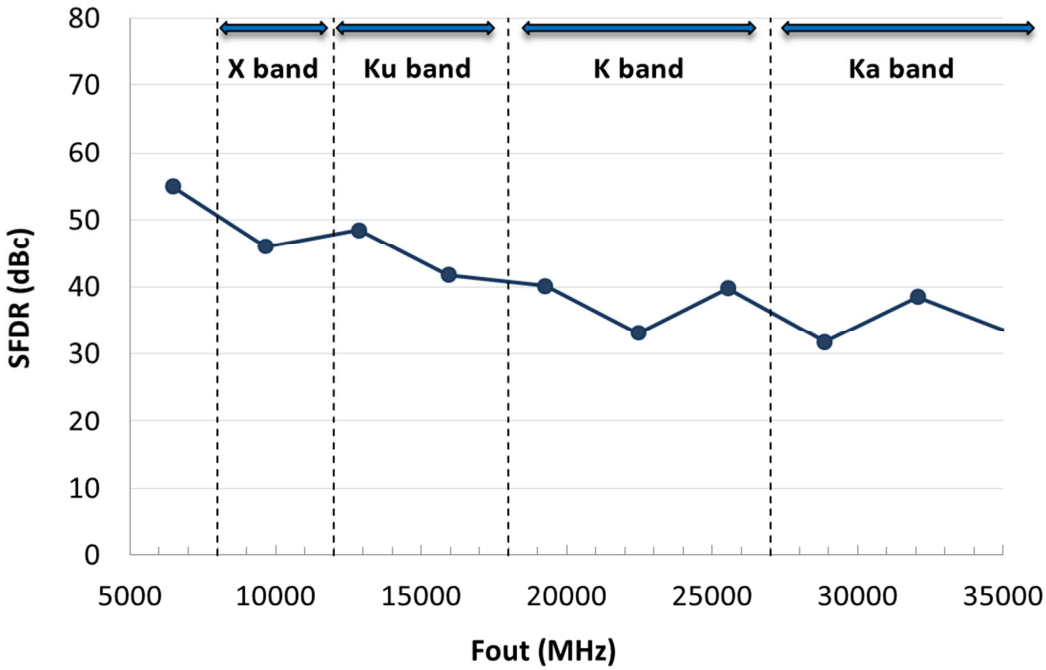


Figure 51. SFDR (dBc) vs Fout from 5 GHz to 35 GHz (covering X-Band, Ku-Band, K-Band and Ka-Band) @ 6.4 GSps in MUX4:1, RF mode



6.2.3 Single Tone Spectrum versus Fout and Output Modes

6.2.3.1 MUX 4:1 at 6.4 GSps

Following figures are given with optimum RPB/RPW settings

Figure 52. Typical SFDR spectrum in NRTZ mode with Fout = 3136 MHz (1st Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 60 dBc

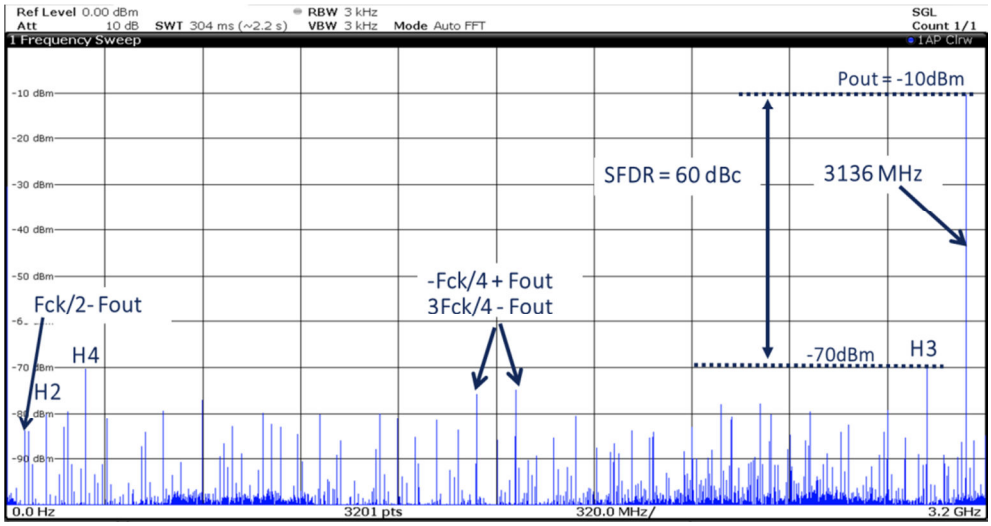


Figure 53. Typical SFDR spectrum in NRTZ mode with Fout = 6336 MHz (2nd Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 53 dBc

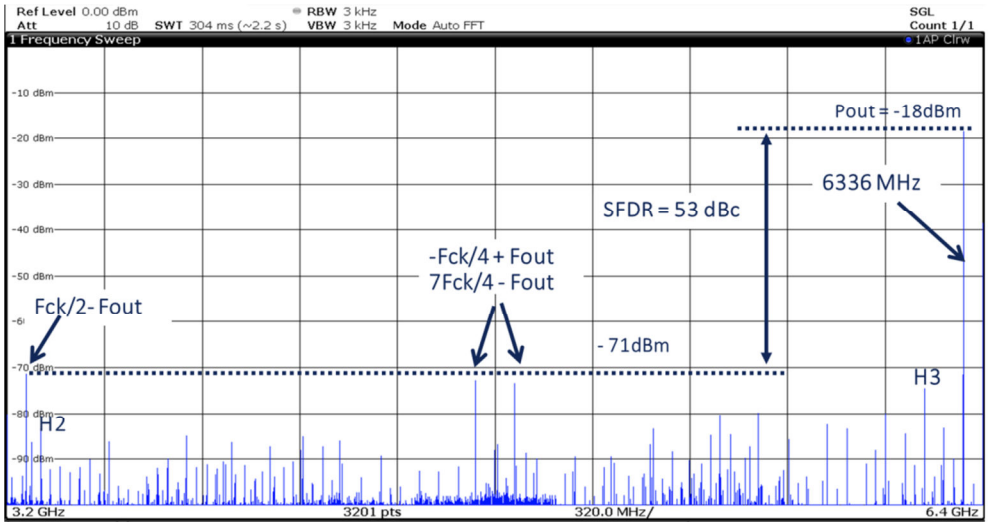


Figure 54. Typical SFDR spectrum in RF mode with Fout = 9536 MHz (3rd Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 50 dBc

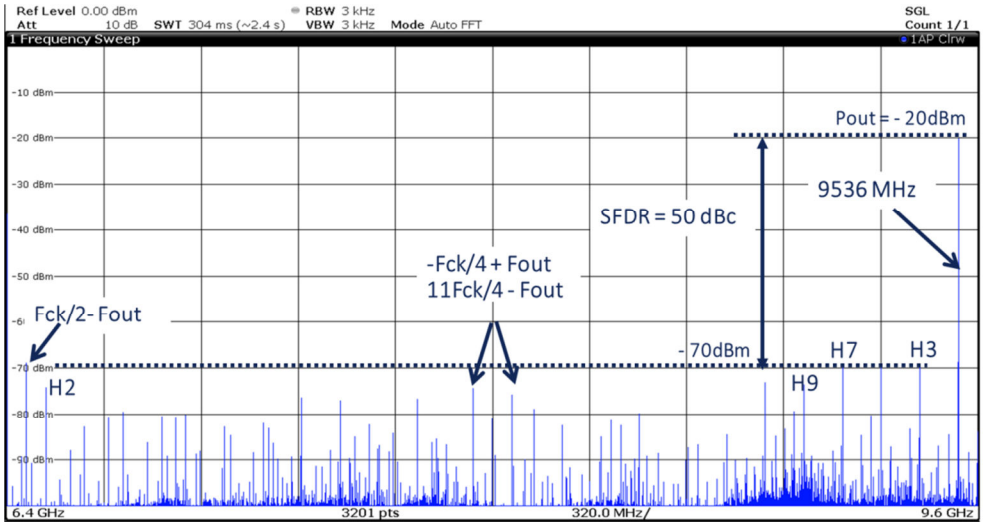


Figure 55. Typical SFDR spectrum in RF mode with Fout = 12736 MHz (4th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 47 dBc

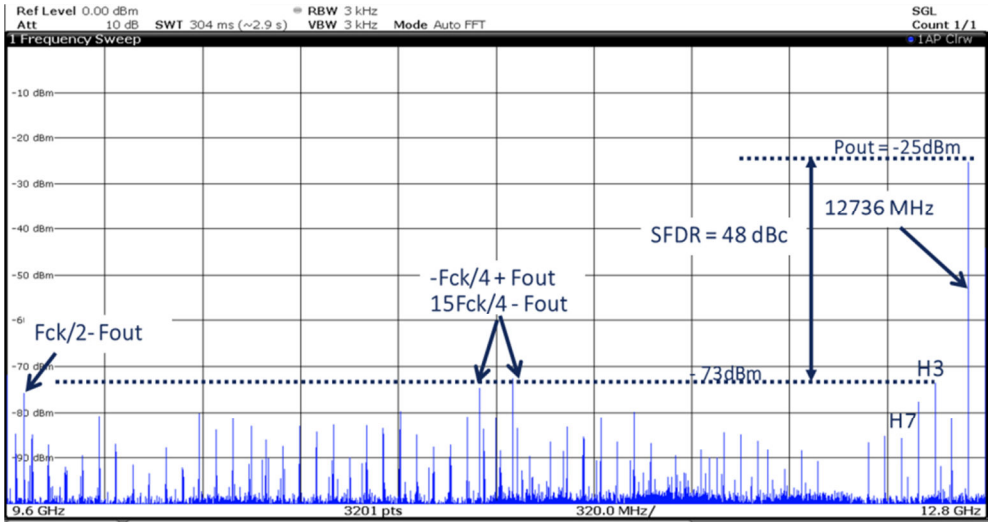


Figure 56. Typical SFDR spectrum in NRTZ mode with Fout = 15936 MHz (5th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 37 dBc

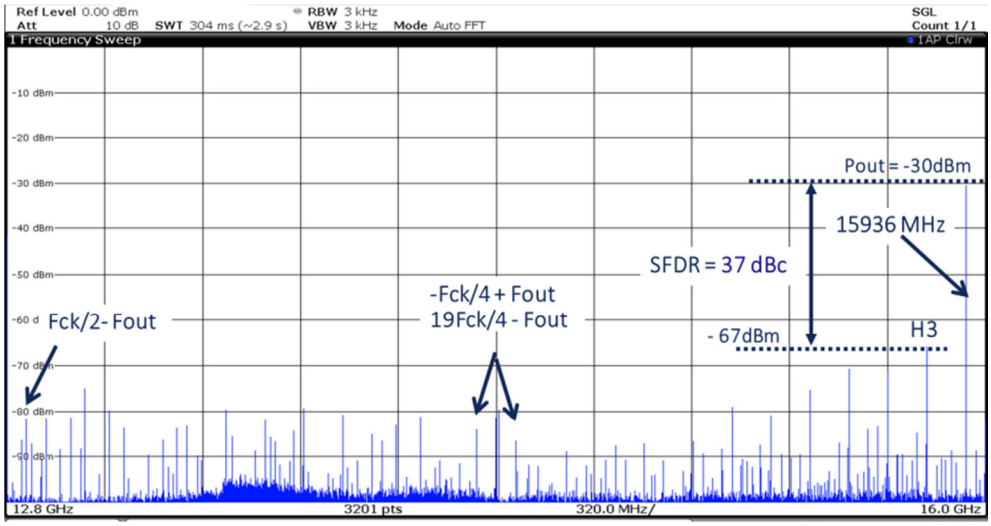


Figure 57. Typical SFDR spectrum in RF mode with Fout = 19146 MHz (6th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 40 dBc

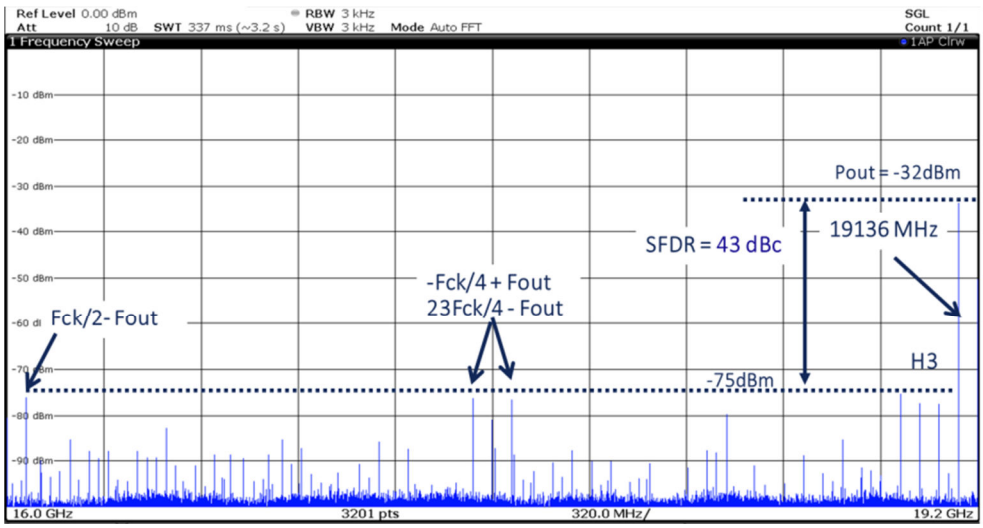


Figure 58 Typical SFDR spectrum in RF mode with Fout = 22336 MHz (7th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 34 dBc

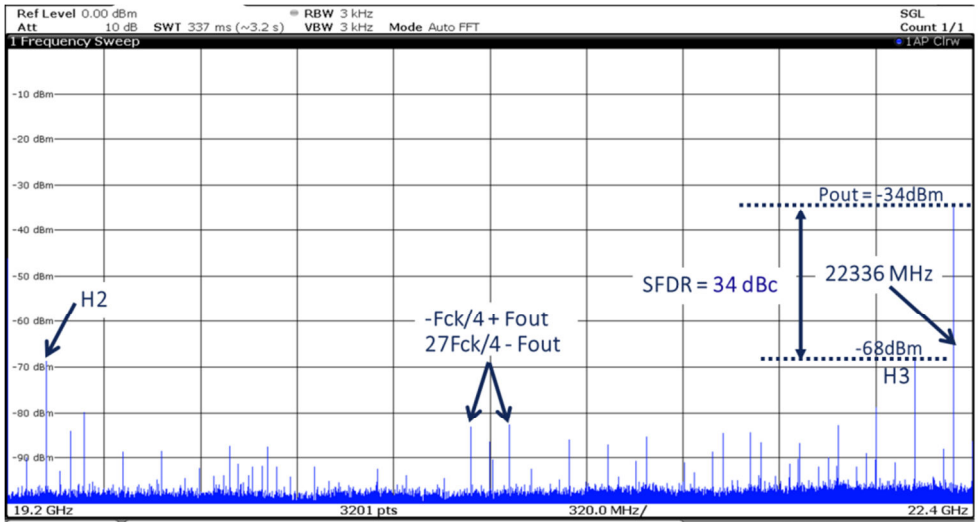
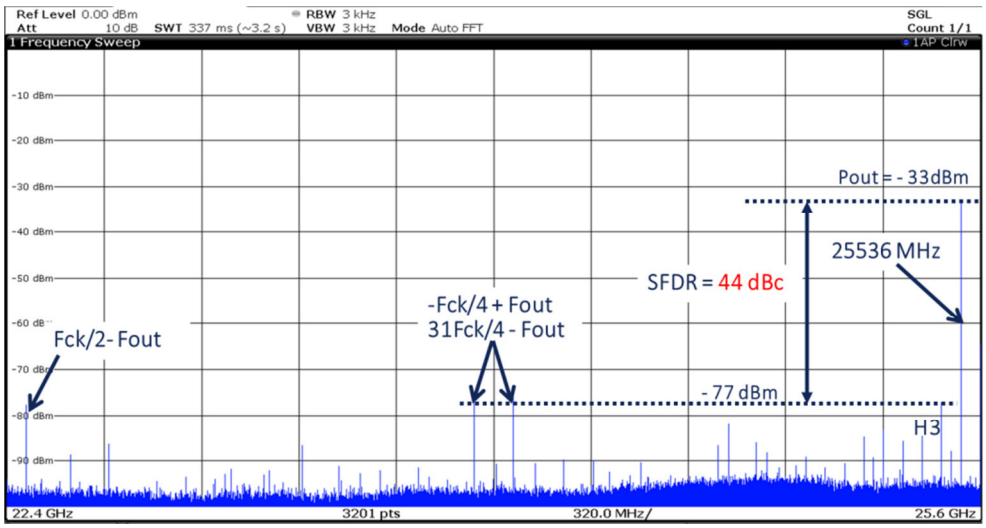


Figure 59 Typical SFDR spectrum in RF mode with Fout = 25536 MHz (8th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 44 dBc



6.2.3.2 MUX 4:1 at 7.0 GSps

Following figures are given with optimum RPB/RPW settings

Figure 60. Typical SFDR spectrum in NRTZ mode with Fout = 3430 MHz (1st Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 55 dBc

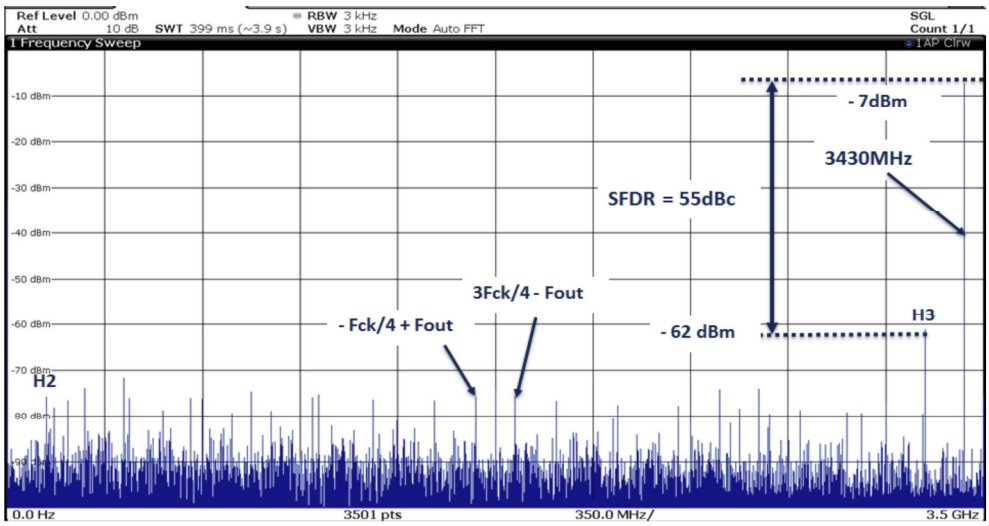


Figure 61. Typical SFDR spectrum in RF mode with Fout = 6930 MHz (2nd Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 58 dBc

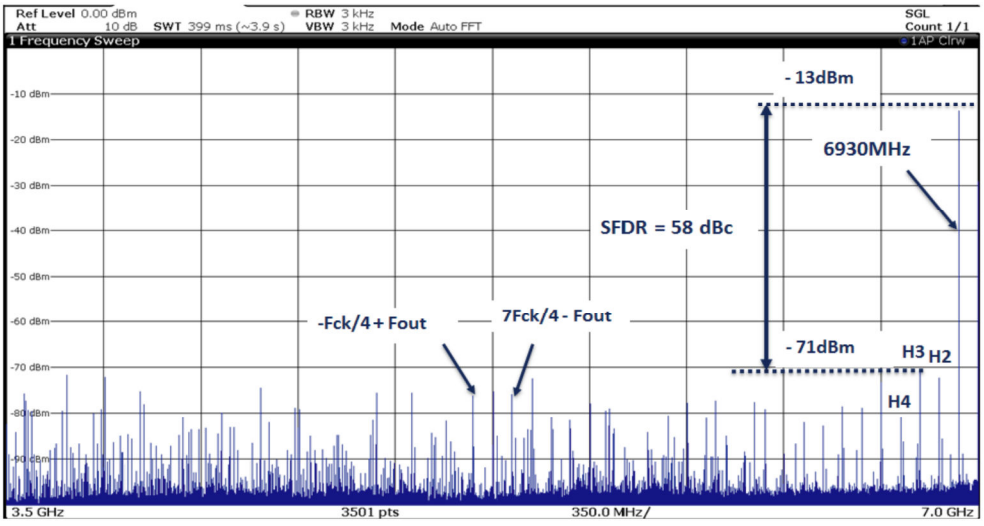


Figure 62. Typical SFDR spectrum in RF mode with Fout = 10430 MHz (3rd Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 50 dBc

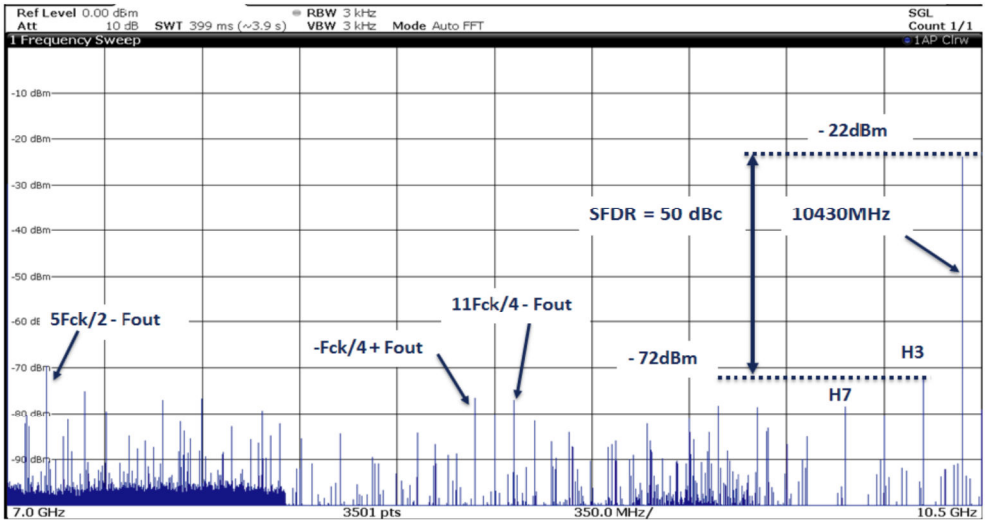


Figure 63. Typical SFDR spectrum in RF mode with Fout = 13930 MHz (4th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 48 dBc

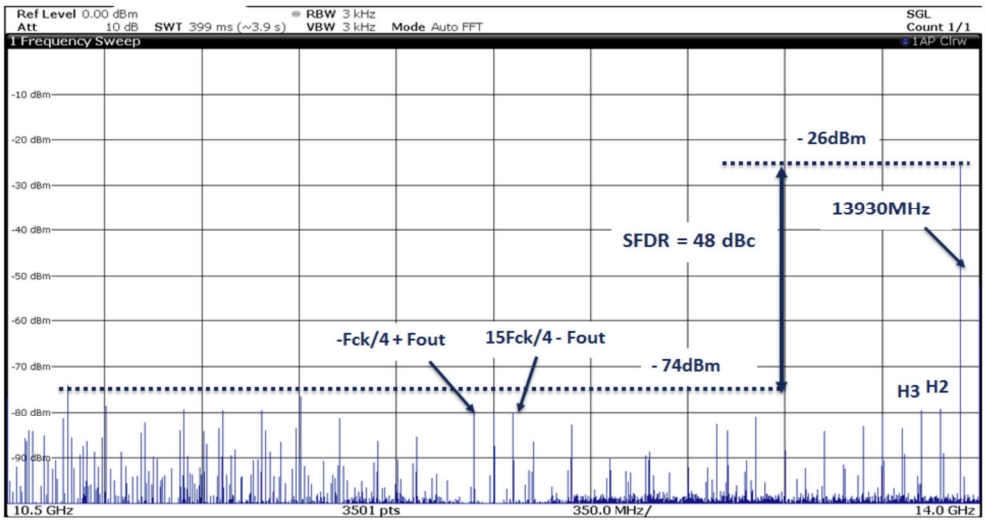


Figure 64. Typical SFDR spectrum in RF mode with Fout = 17430 MHz (5th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 41 dBc

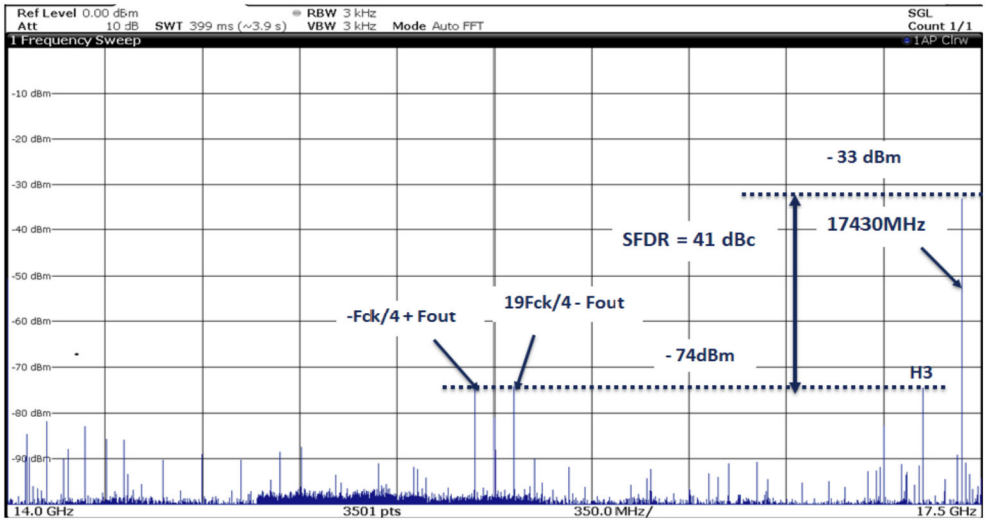


Figure 65. Typical SFDR spectrum in RF mode with Fout = 20930 MHz (6th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 36 dBc

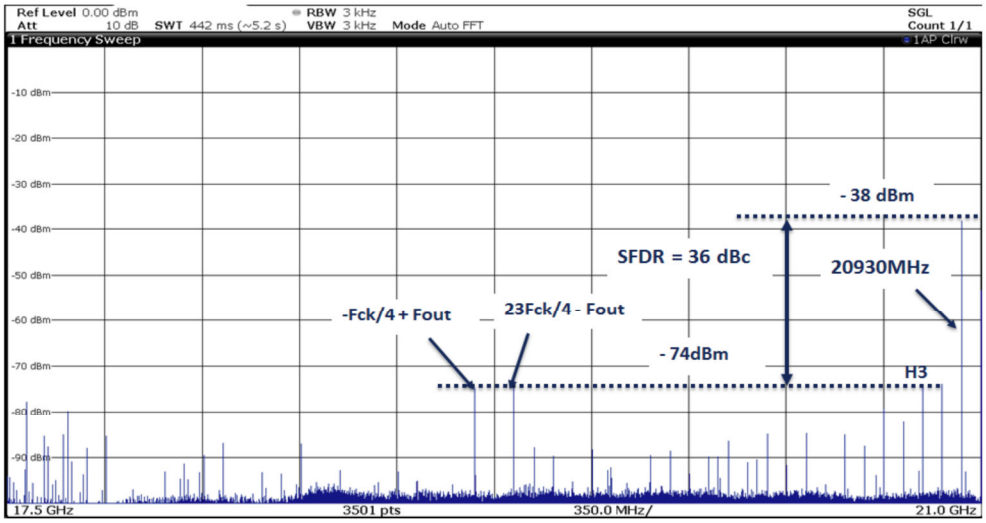
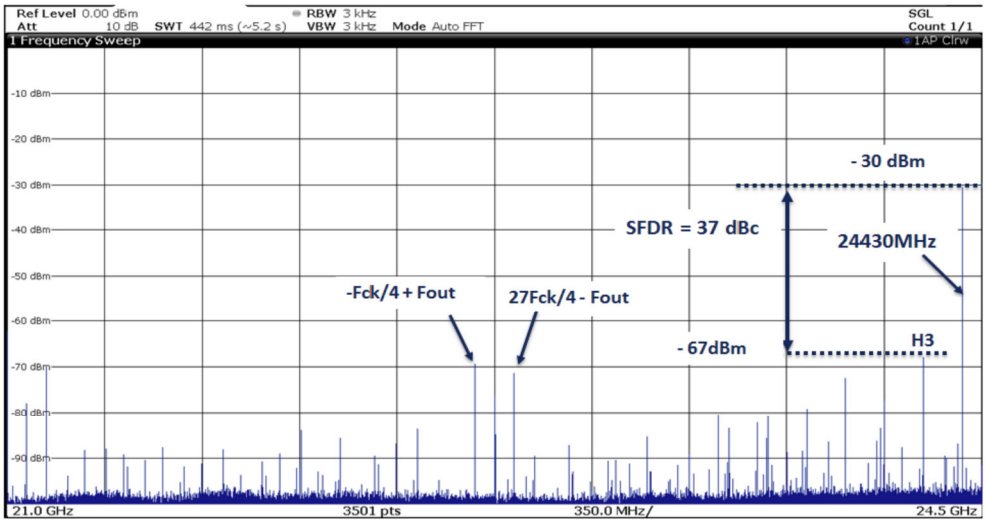


Figure 66. Typical SFDR spectrum in RF mode with Fout = 24430 MHz (7th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 37 dBc



6.2.3.3 MUX 4:1 at 8.0 GSps in IUCM2 Mode in NZ4 and NZ5

Figure 67. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ4 (Fout = 6040MHz) and (Fout=7960MHz), Fs = 8.0 GSps

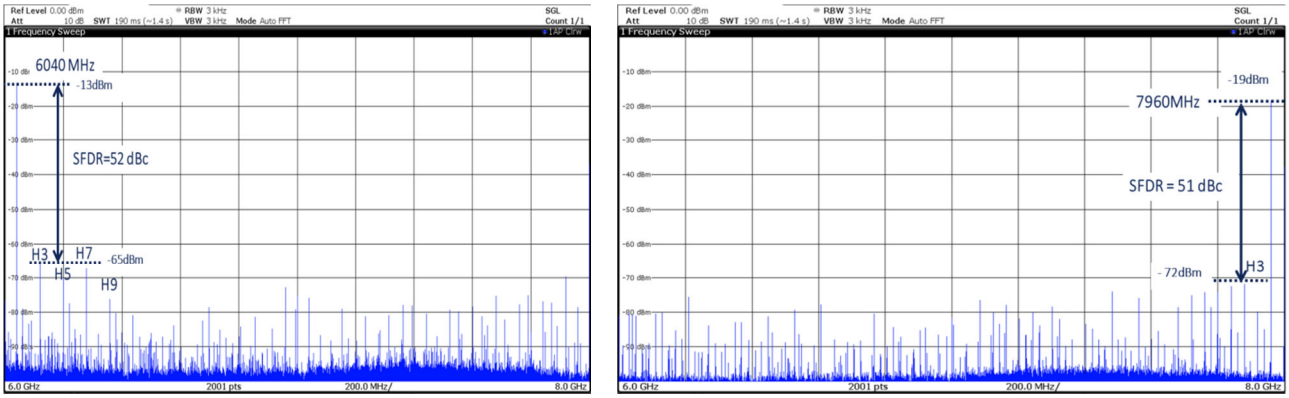
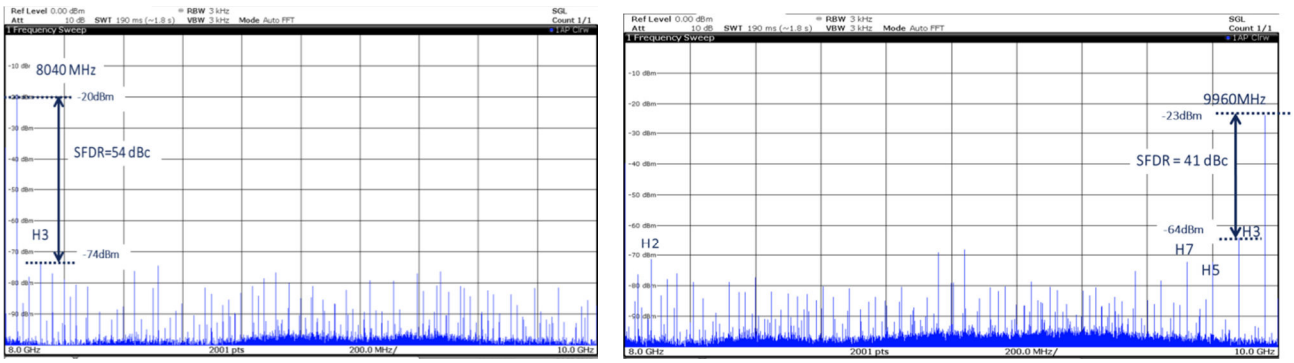


Figure 68. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ5 (Fout = 8040 MHz) and Fout = 9960 MHz, Fs = 8.0 GSps



6.2.3.4 MUX 4:1 at 8.0 GSps IUCM4 Mode in NZ8 and NZ9

Figure 69. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ8 (Fout = 7020 MHz) and (Fout = 7980 MHz), Fs = 8.0 GSps

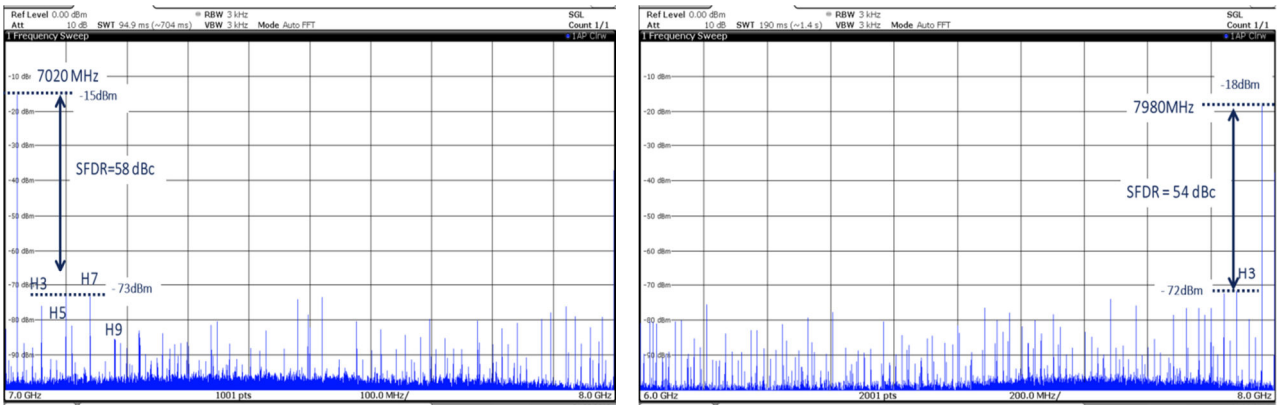
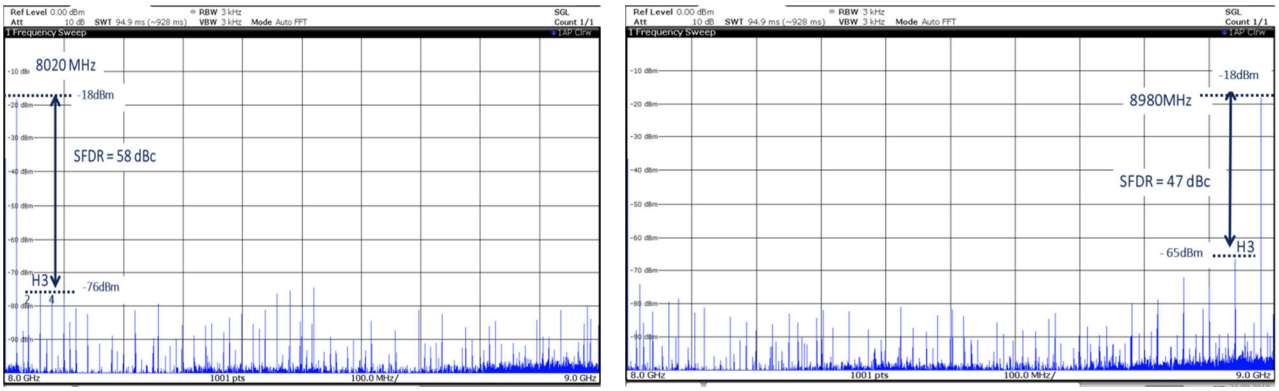


Figure 70. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ9 (Fout = 8020 MHz) and (Fout = 8980MHz), Fs = 8.0 GSps



6.2.3.6 MUX 4:1 at 8.5 GSps IUCM2 Mode in NZ4 and NZ5

Figure 71. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ4 (Fout = 6417 MHz) and (Fout = 7960 MHz), Fs = 8.5 GSps

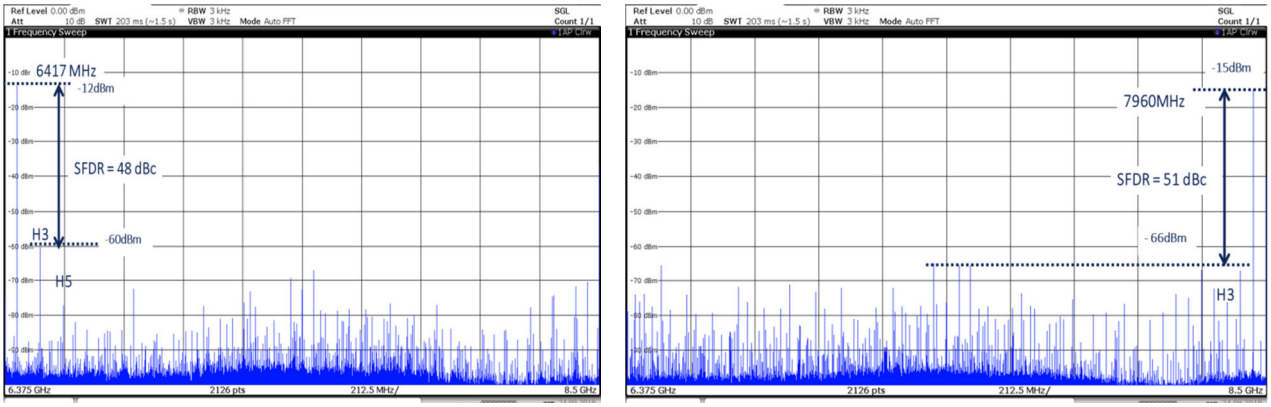
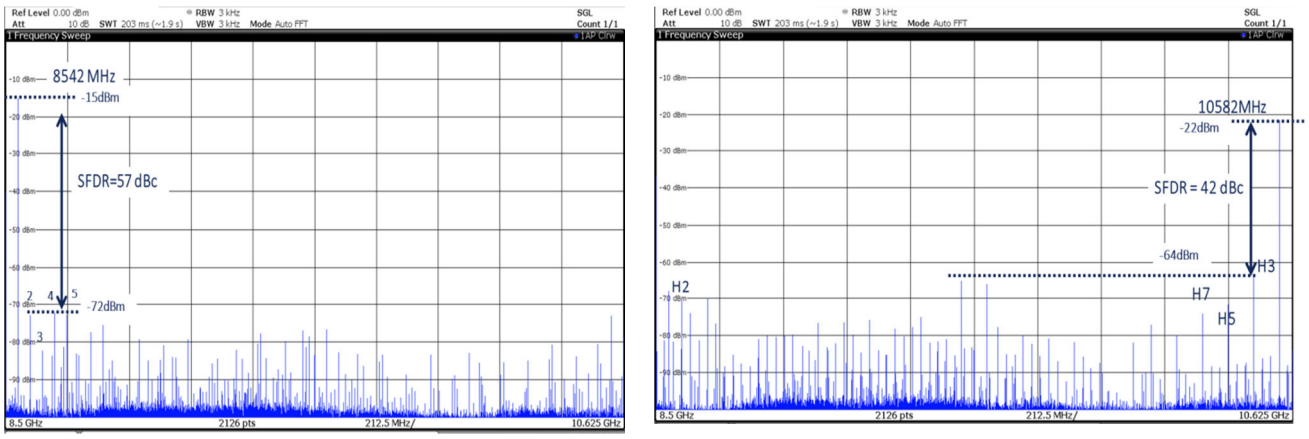


Figure 72. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ5 (Fout = 8542 MHz) and (Fout = 10582 MHz), Fs = 8.5 GSps



6.2.3.7 MUX 4:1 at 8.5 GSps IUCM4 Mode in NZ8 and NZ9

Figure 73. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ8 (Fout = 7458 MHz) and (Fout = 8478 MHz), Fs = 8.5 GSps

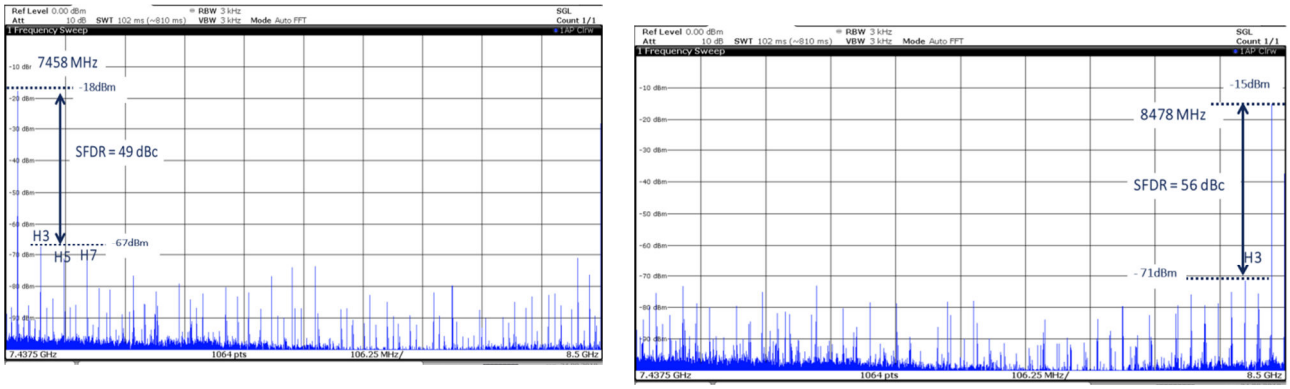
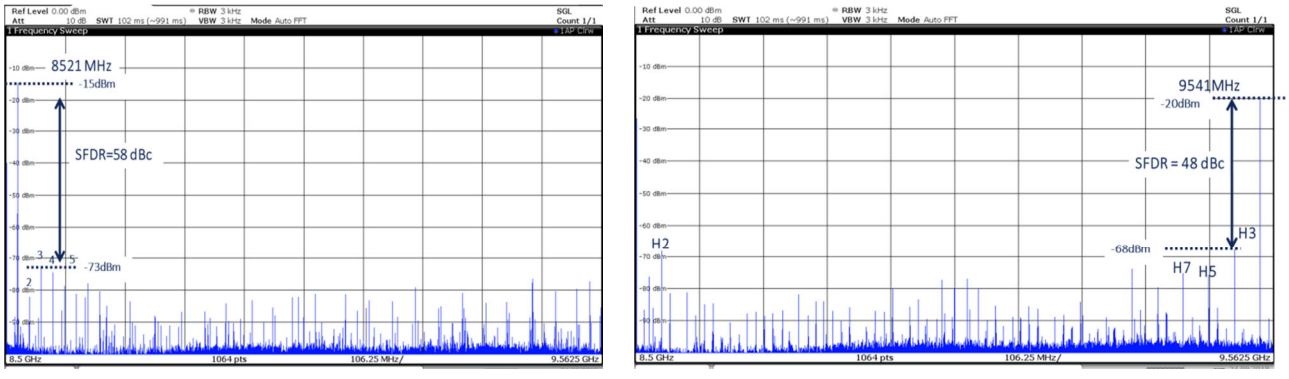


Figure 74. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ9 (Fout = 8521 MHz) and (Fout = 9541 MHz), Fs = 8.5 GSps



6.2.3.8 MUX 2:1 at 3.2 GSps

Figure 75. Typical SFDR spectrum in NRZ mode. Fout = 32 MHz (1st Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 70 dBc

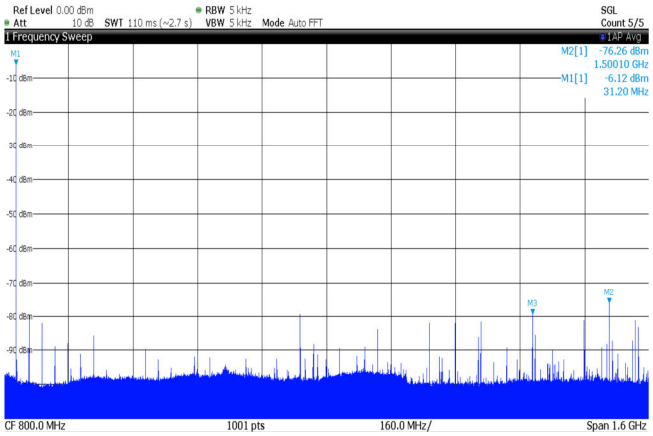


Figure 76. Typical SFDR spectrum in NRTZ mode. Fout = 32 MHz (1st Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 76 dBc

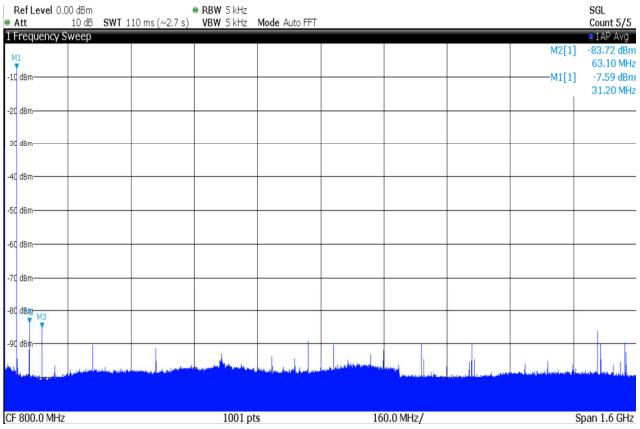


Figure 77.Typical SFDR spectrum in NRTZ mode. Fout = 1568 MHz (1st Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 65 dBc

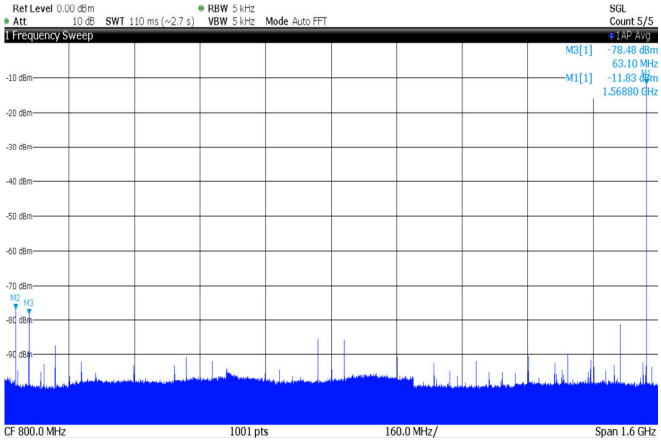


Figure 78. Typical SFDR spectrum in RTZ mode. Fout = 3168 MHz (2nd Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 59 dBc

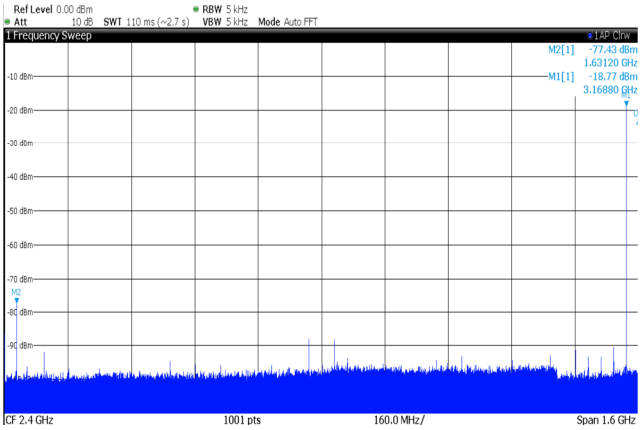


Figure 79. Typical SFDR spectrum in RF mode. Fout = 3168 MHz (2nd Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 58 dBc

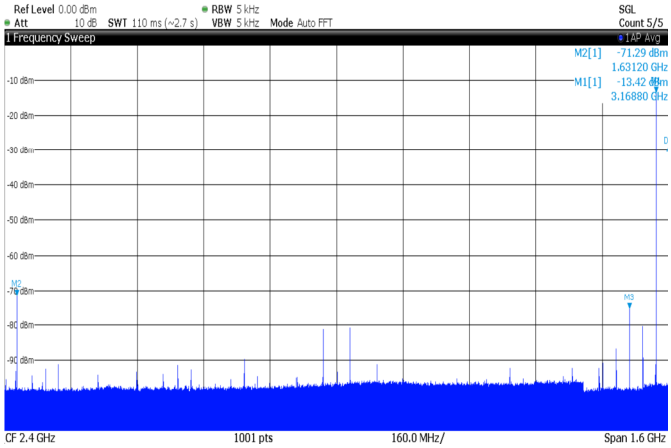
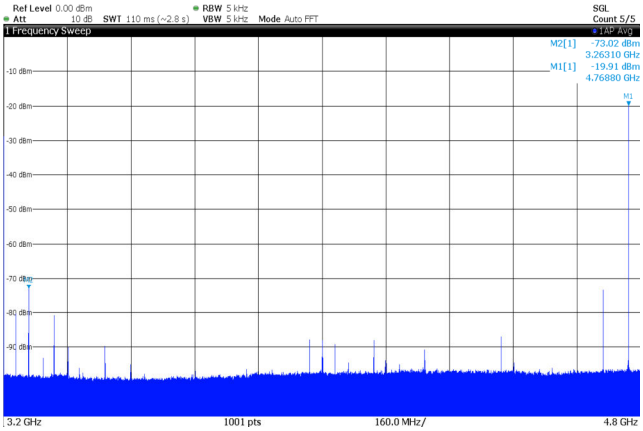


Figure 80. Typical SFDR spectrum in RF mode. Fout = 4768 MHz (3rd Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 53 dBc



6.2.4 Single Tone SFDR Measurements versus Fclock (MUX 4:1)

The following figures show typical SFDR performance of an EV12DS480A device versus sampling rate. RPB and RPW settings are set in order to maximize SFDR values (RPB and RPW parameters are therefore not constant versus Fclk).

Figure 81. SFDR versus Fclk in 1st Nyquist zone for 4 output modes.
Fout = Fclk/2 - Fclk/100

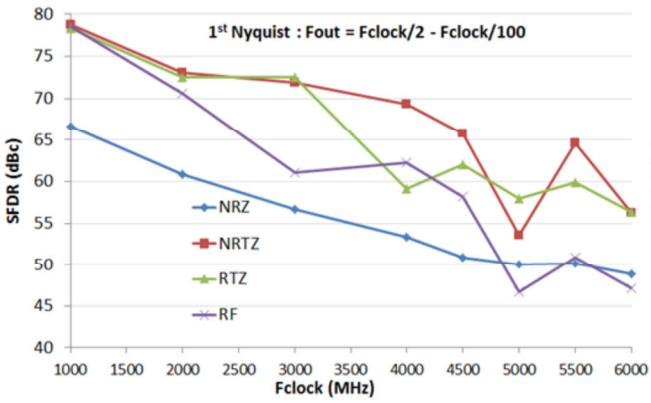
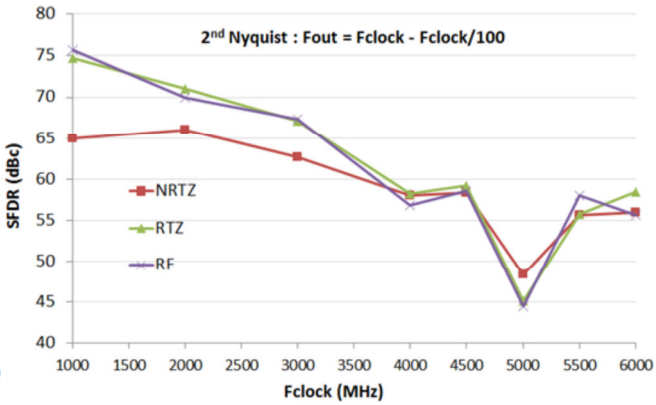


Figure 82. SFDR versus Fclk in 2nd Nyquist zone for 3 output modes.
Fout = Fclk - Fclk/100



6.2.5 SFDR vs Power supplies & Temperature

Figure 83. SFDR vs Power supplies vs modes

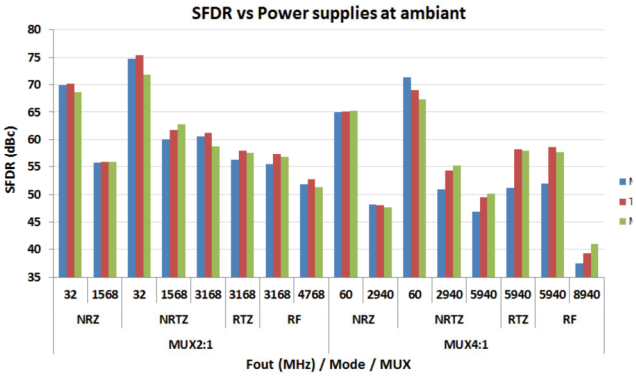
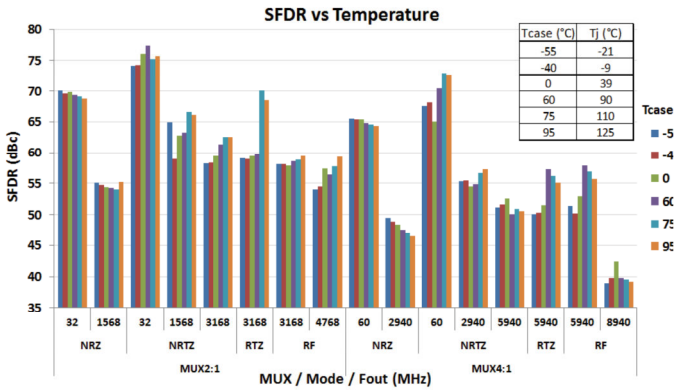


Figure 84. SFDR vs temperature vs modes



6.2.6 Dual Tones Spectra

6.2.6.1 Dual-tone Spectra at 6.4 GSps

Following figures are given with optimum RPB/RPW settings to minimize IMD3- to IMD9- levels.

Figure 85. Typical Dual-tone IMD3- to IMD9- (highest spur) versus (Fout1, Fout2) from 6000 MHz to 23000MHz, Fs = 6.4 GSps, (Fout1-Fout2 =10MHz apart) in RF mode

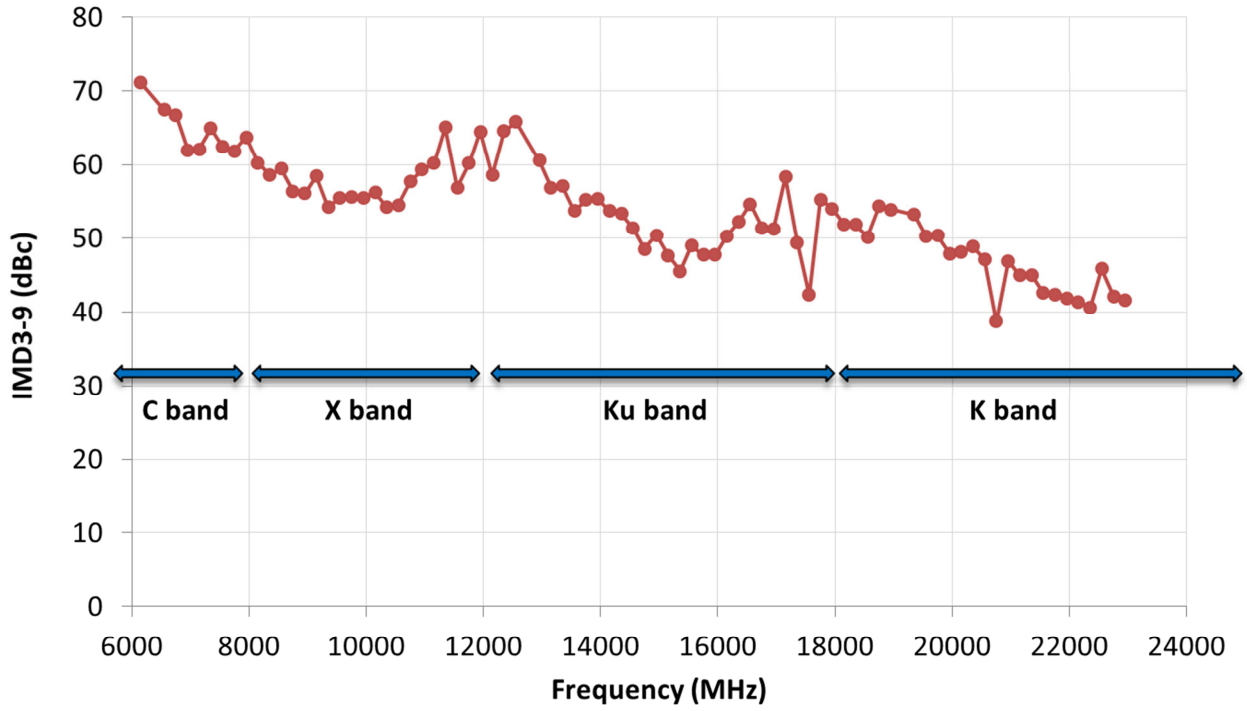


Figure 86. Typical Dual-tone spectrum in NRTZ mode with Fout1,Fout2 = 2950 MHz,2960 MHz (1st Nyquist), MUX4:1, Fs = 6.4 GSps, IMD3 - = 70 dBc, IMD full Nyquist = 50 dBc

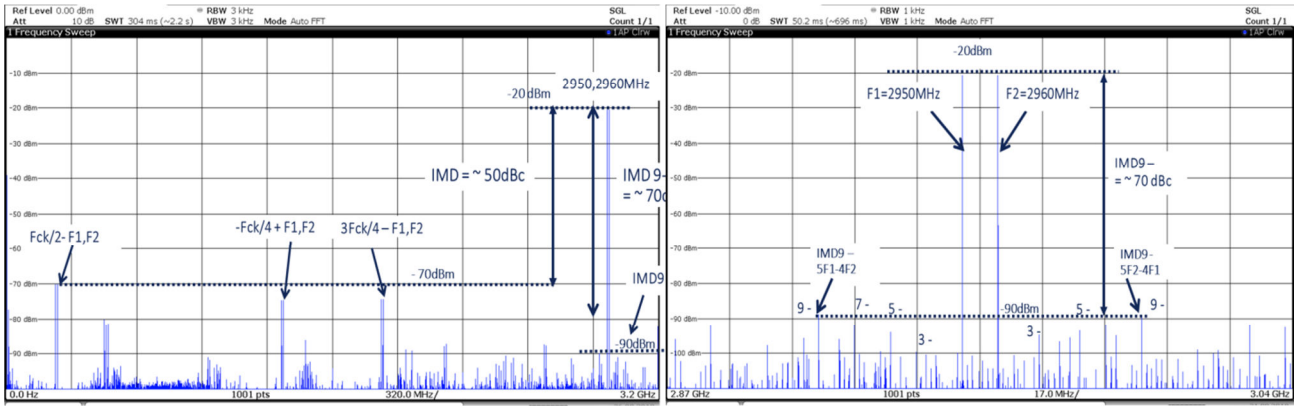


Figure 87. Typical Dual-tone spectrum in RF mode with Fout1, Fout2 = 6150 MHz,6160 MHz, (2nd Nyquist), MUX4:1, Fs = 6.4 GSps, IMD7 - = 67 dBc, IMD full Nyquist = 44 dBc

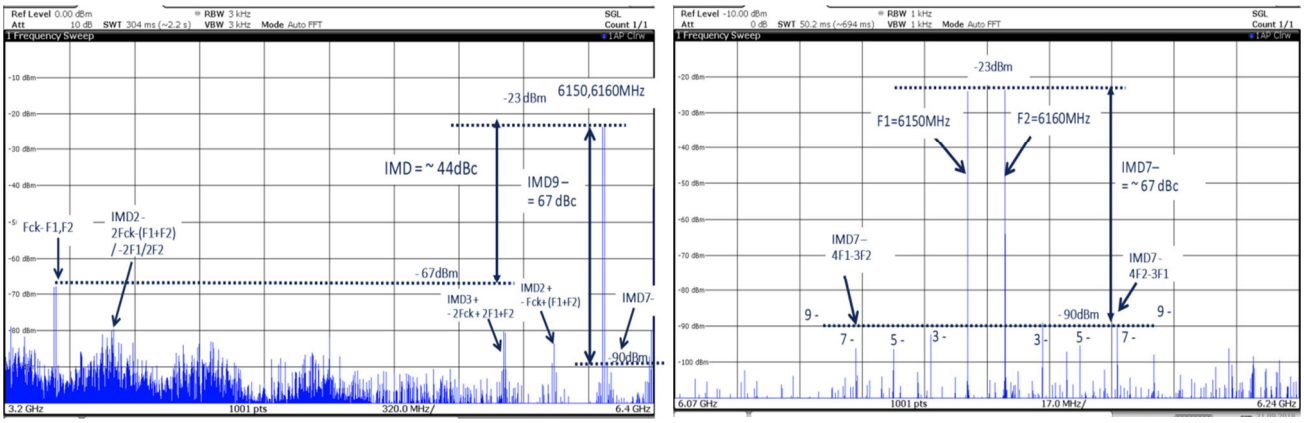


Figure 88. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 9150 MHz,9160 MHz (3rd Nyquist), MUX4:1, Fs = 6.4 GSps, IMD5 - = 55 dBc, IMD full Nyquist = 44 dBc

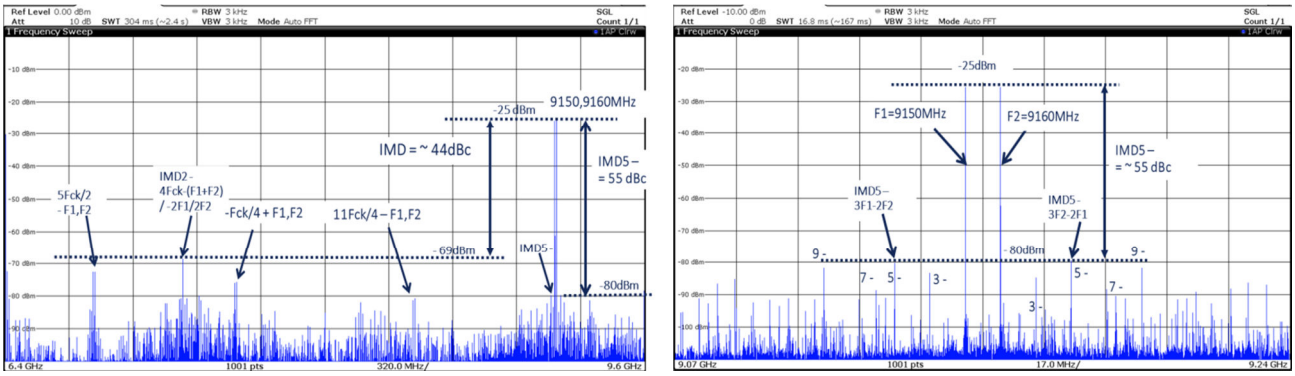
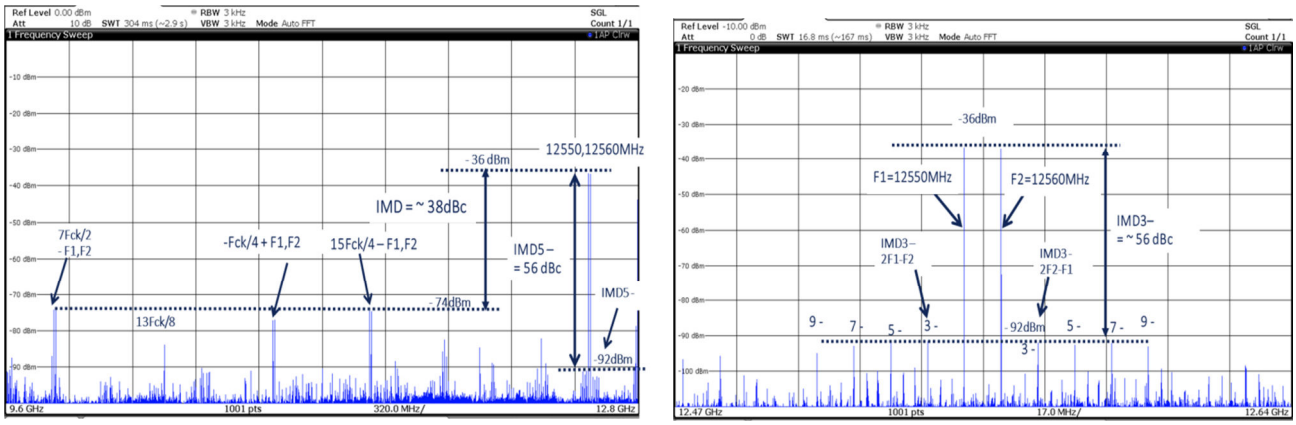


Figure 89. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 12550 MHz,12560 MHz (4th Nyquist), MUX4:1, Fs = 6.4 GSps, IMD3 - = 56 dBc, IMD full Nyquist = 38 dBc



6.2.6.2 Dual-tone Spectra at 7.0 GSps

Following figures are given with optimum RPB/RPW settings.

Figure 90. Typical Dual-tone spectrum in NRTZ mode with Fout1,Fout2 = 3450 MHz, 3460 MHz (1st Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 53 dBc, IMD full Nyquist = 51 dBc

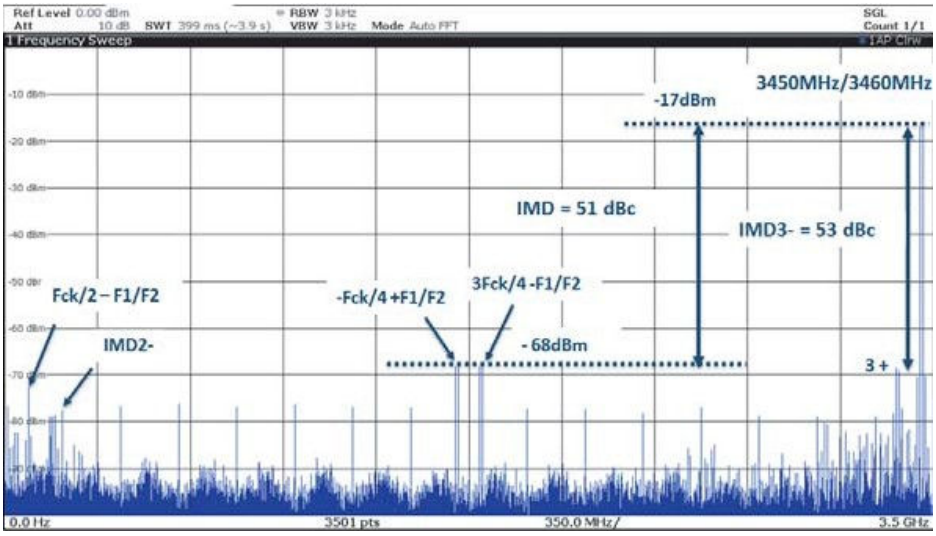


Figure 91. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 6950 MHz,6960 MHz (2nd Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 64 dBc, IMD full Nyquist = 59 dBc

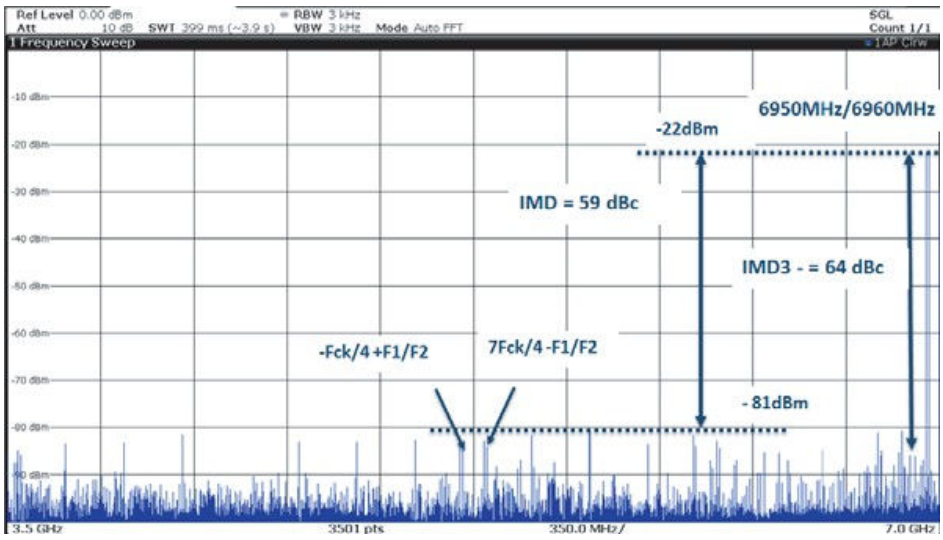


Figure 92. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 10450 MHz,10460 MHz (3rd Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 52 dBc, IMD full Nyquist = 44 dBc

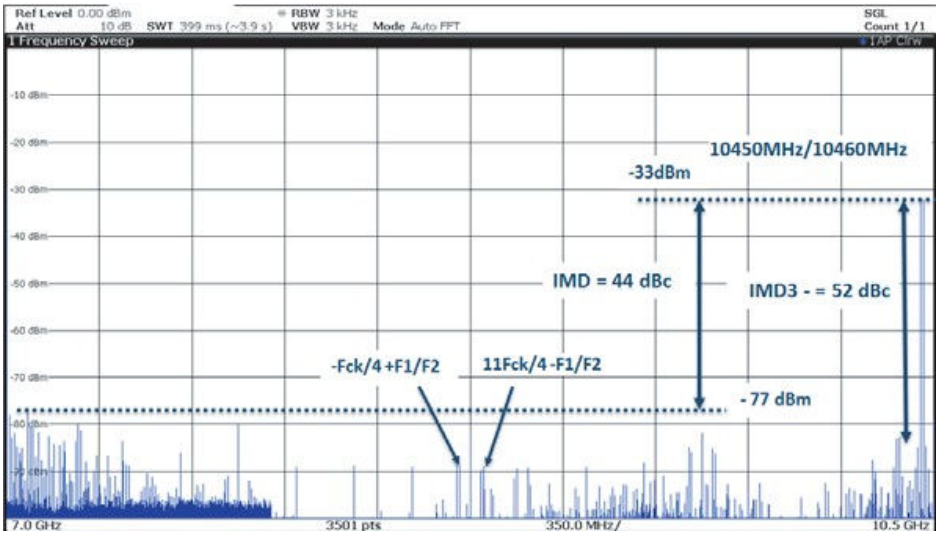
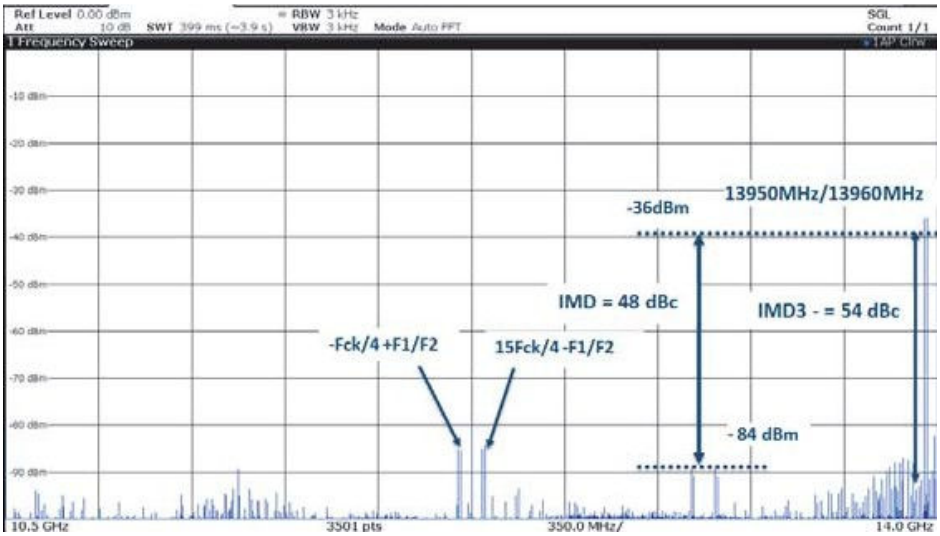


Figure 93. Typical Dual-tone spectrum in NRTZ mode with Fout1,Fout2 = 13950 MHz,13960 MHz, (4th Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 54 dBc, IMD full Nyquist = 48 dBc



6.2.7 ACPR measurements @ 6.0 GSps (10 MHz QPSK)

Figure 94. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 1.6 GHz Center frequency, ACPR = 59 dBc, NRTZ mode

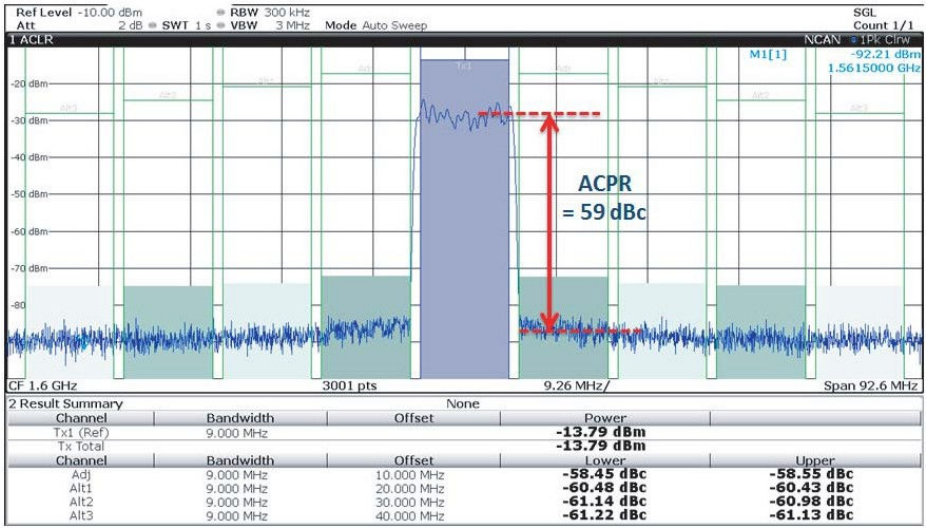


Figure 95. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 4.6 GHz Center frequency, ACPR = 52 dBc, NRTZ mode

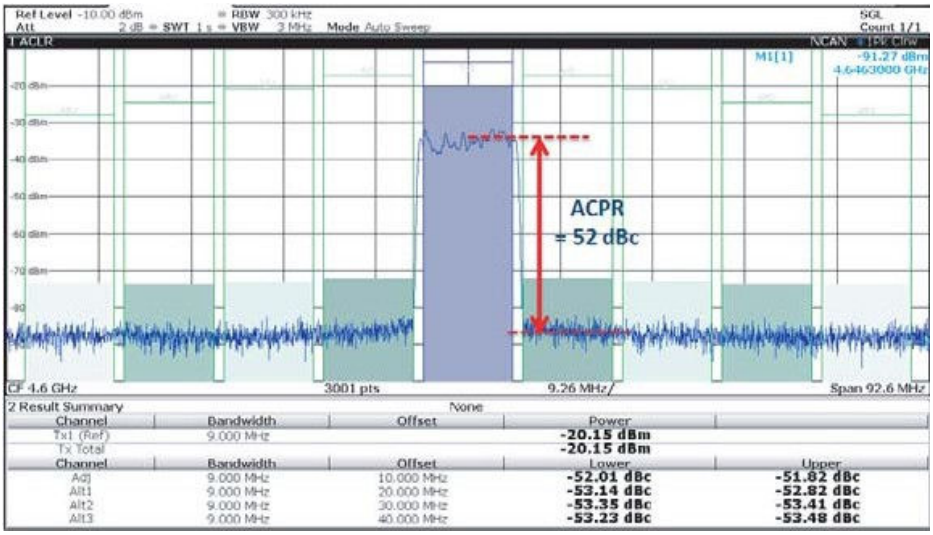


Figure 96. Adjacent Channel Power Ratio (ACPR)@ 6.0 GSps, 10 MHz QPSK, 10.6 GHz Center frequency, ACPR = 42 dBc, RF mode

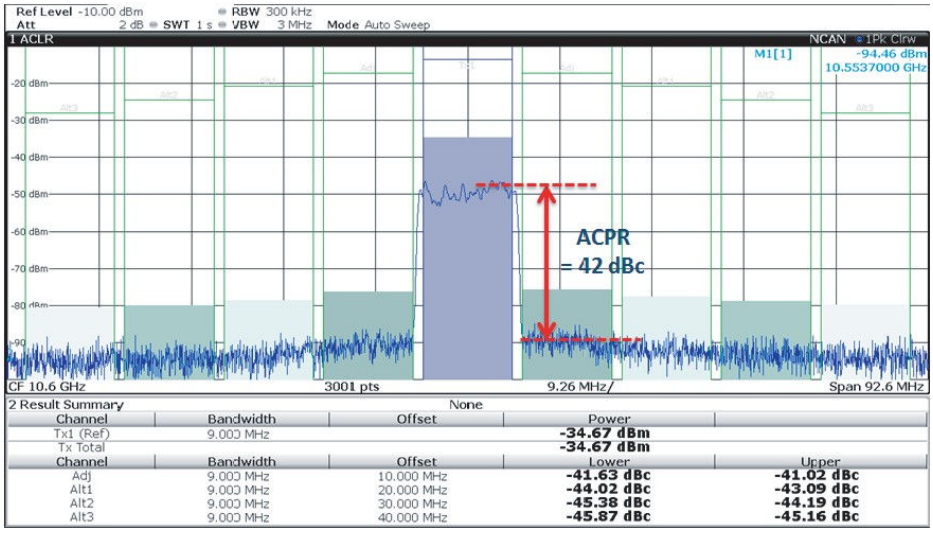


Figure 97. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 16.6 GHz Center frequency, ACPR = 36.7 dBc, RF mode

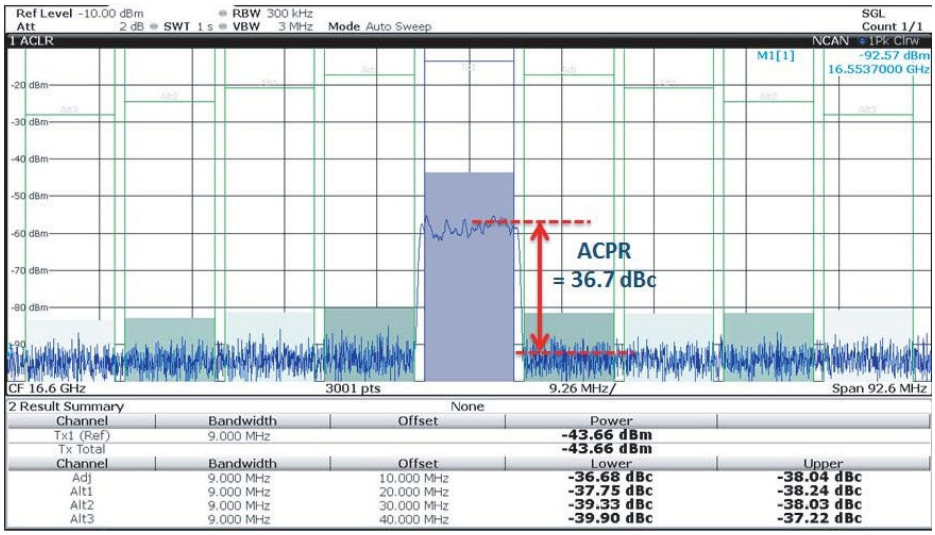


Figure 98. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 22.6 GHz Center frequency, ACPR = 30 dBc, RF mode

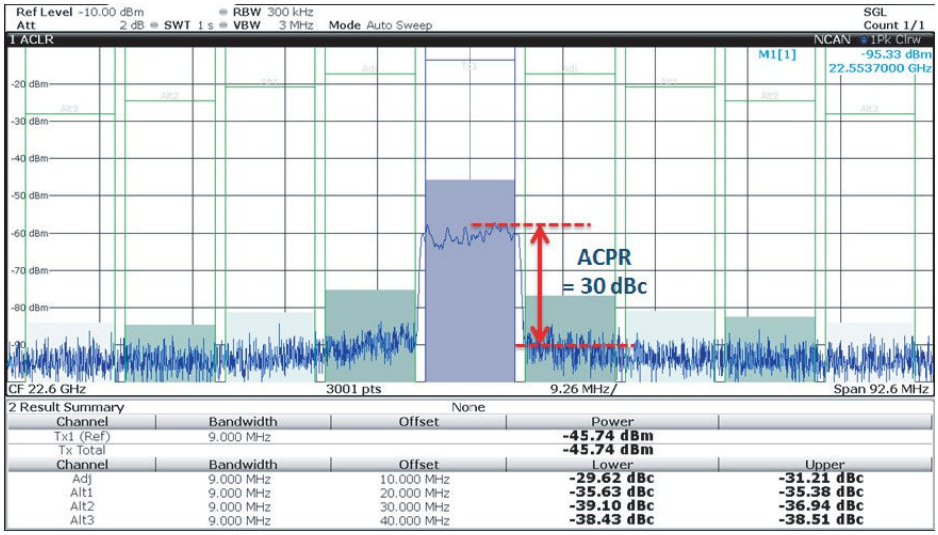
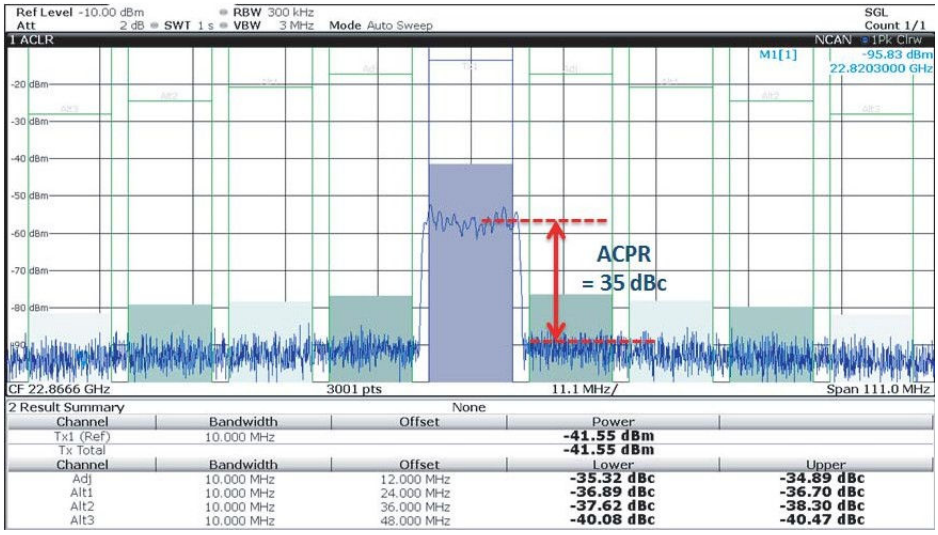


Figure 99. Adjacent Channel Power Ratio (ACPR) @ 7.0 GSps, 10 MHz QPSK, 22.9 GHz Center frequency, ACPR = 35 dBc, RF mode

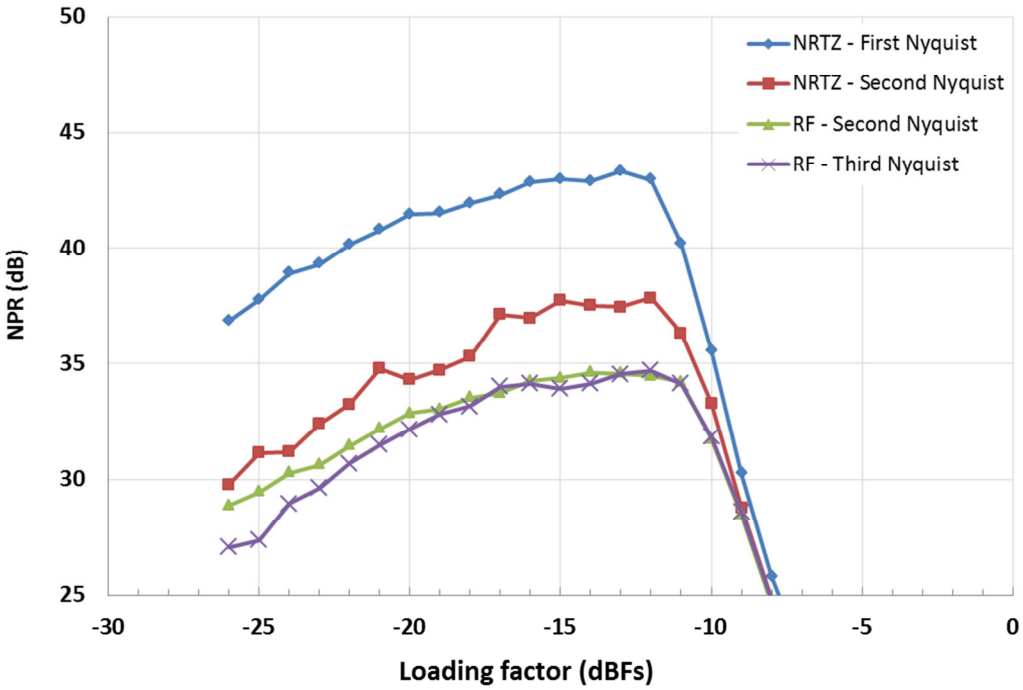


6.2.8 NPR performance

6.2.8.1 NPR vs Loading Factor (LF)

NPR pattern covers a 2880 MHz bandwidth (90% of 3200MHz Nyquist zone) with a 60 MHz notch width centered at the middle of the Nyquist zone.

Figure 100. NPR versus Loading Factor @ 6.4 Gsps (optimum NPR value is achieved for LF = –14 dBFS)



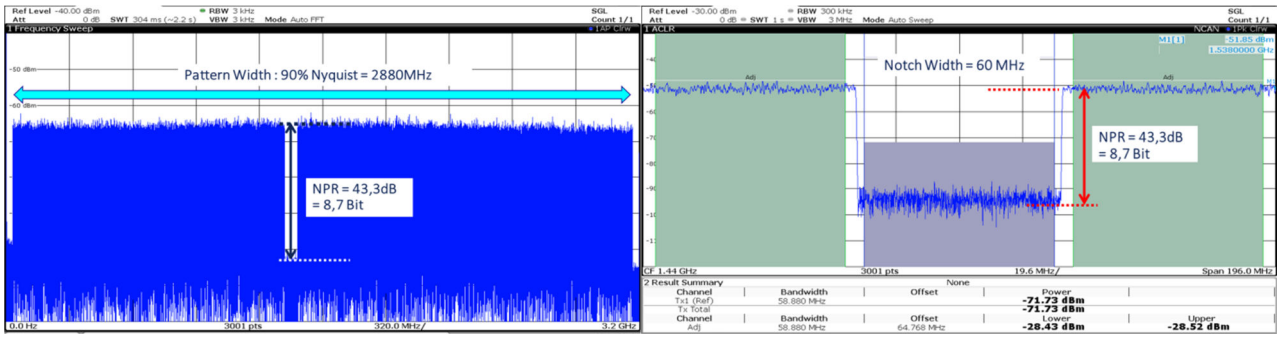
6.2.8.2 NPR over 3 Nyquist zones versus mode

NPR measurements have been carried out at optimum loading factor (LF) for a 12 bit DAC, that is –14 dBFS.

SNR can be computed from NPR measurement with the formula: SNR[dB] = NPR[dB] + ILF[dB]I – 3 = NPR+11dB.
ENOB can be computed with the formula: ENOB = (SNR[dB] - 1.76) / 6.02.

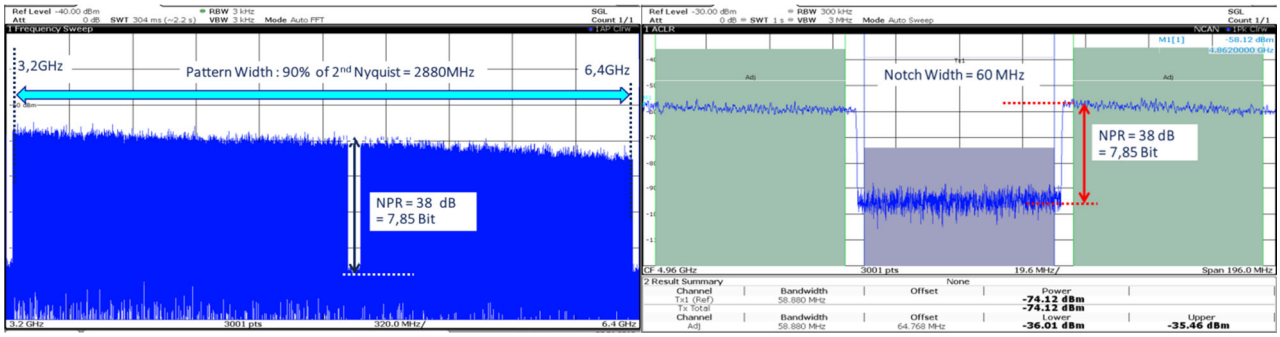
6.2.8.2.1 NPR at 6.4 GSps

Figure 101. NPR in 1st Nyquist Zone, NRTZ mode, DC to 3200MHz, 90% Nyquist = 2880MHz Noise Pattern with a 60 MHz Notch Centered on 1440 MHz



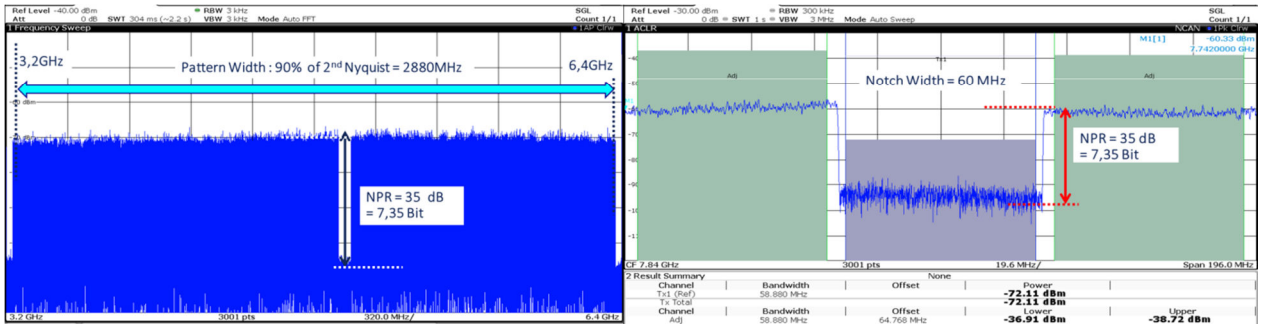
Measured average NPR: 43.5 dB, therefore SNR = 54,3 dB and ENOB = 8.7 bit

Figure 102. NPR in 2nd Nyquist Zone, 3200 MHz to 6400 MHz with 90% Noise Pattern with a 60 MHz Notch Centered on 4960 MHz, NRTZ mode.



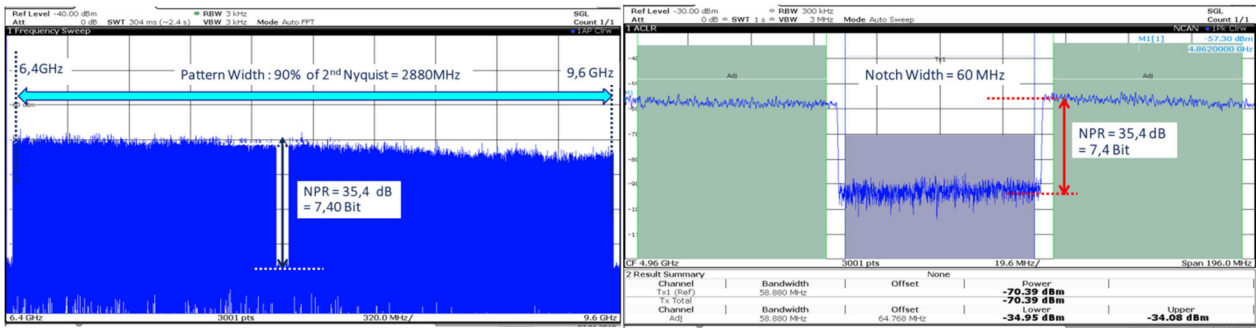
Measured average NPR: 38 dB, therefore SNR = 49 dB and ENOB = 7,85 bit

Figure 103. NPR in 2nd Nyquist Zone, 3200 MHz to 6400 MHz with 90% Noise Pattern with a 60 MHz Notch Centered on 4960 MHz, RF mode.



Measured average NPR: 35 dB, therefore SNR = 46 dB and ENOB = 7.35 bit

Figure 104. NPR in 3rd Nyquist Zone, 6400 MHz to 9600 MHz with 90% Noise Pattern with a 60 MHz Notch Centered on 7840 MHz, RF mode.



Measured average NPR: 35,4 dB, therefore SNR = 46,4 dB and ENOB = 7.4 bit

6.2.8.2.2 NPR at 7.0 GSps

Figure 105. NPR @ 7.0 GSps in 1st Nyquist, 3150 MHz pattern, NPR = 42.6 dB (= 8.6 Bit ENOB), NRTZ mode

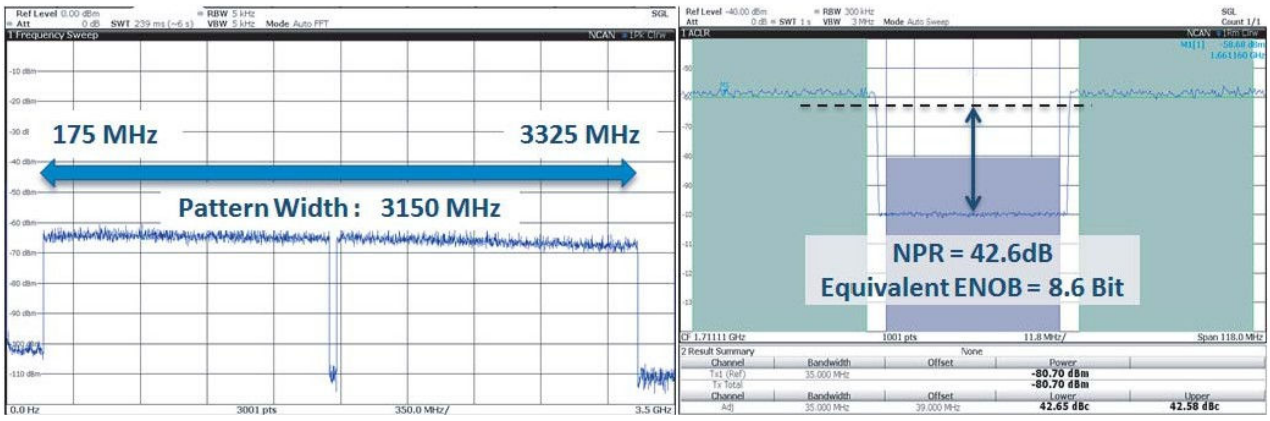


Figure 106. NPR @ 7.0 GSps in 2nd Nyquist, 3150 MHz pattern, NPR = 36.2 dB (= 7.6 Bit ENOB), NRTZ mode

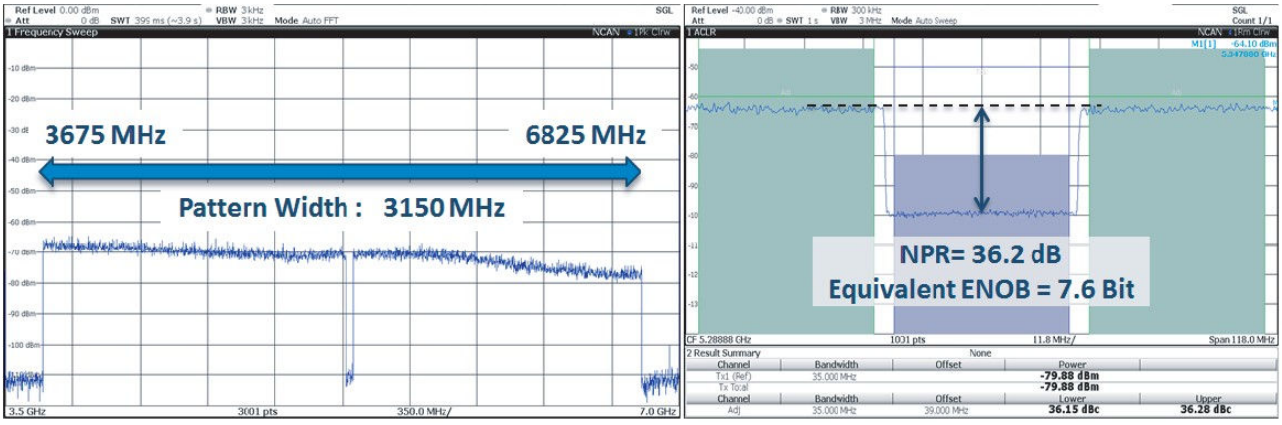
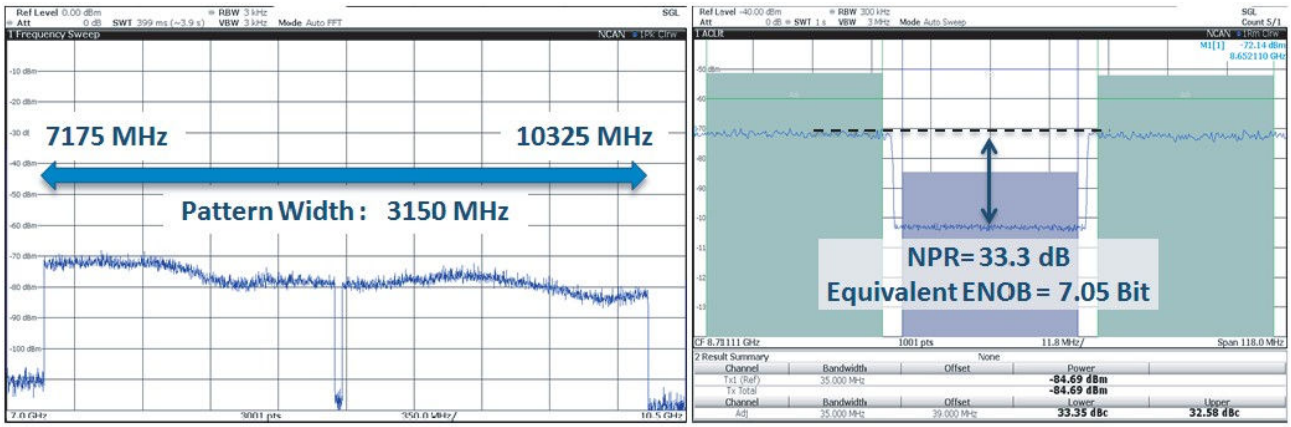


Figure 107. NPR @ 7.0 GSps in 3rd Nyquist, 3150 MHz pattern, NPR = 33.3 dB (= 7.1 Bit ENOB), RF mode

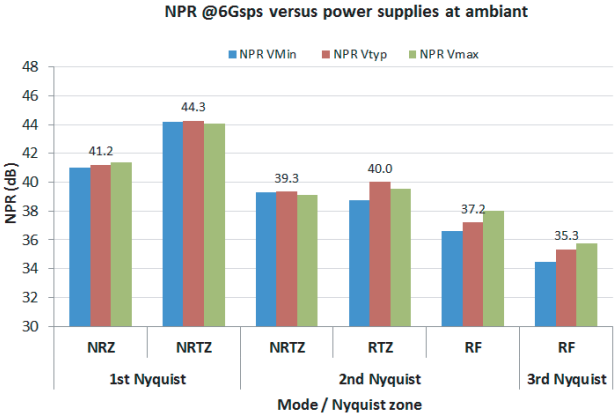


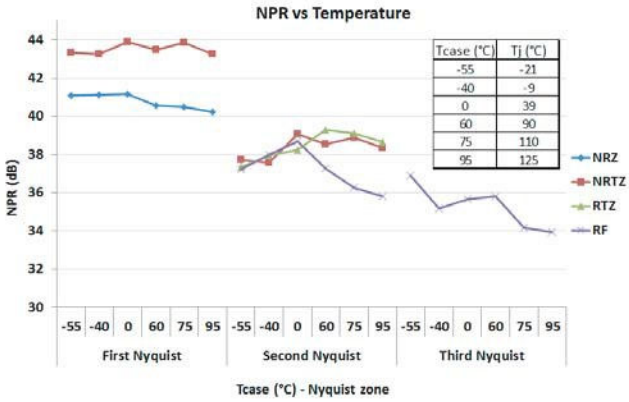
6.2.8.3 NPR vs Power supplies & Temperature

Figure 108. NPR vs power supply in the 4 output modes at room temperature

Figure 109. NPR versus temperature at 6.0 GSps For the 4 output modes from Tc = –55°C to Tc = 95°C (Tj = –21°C to 125°C)

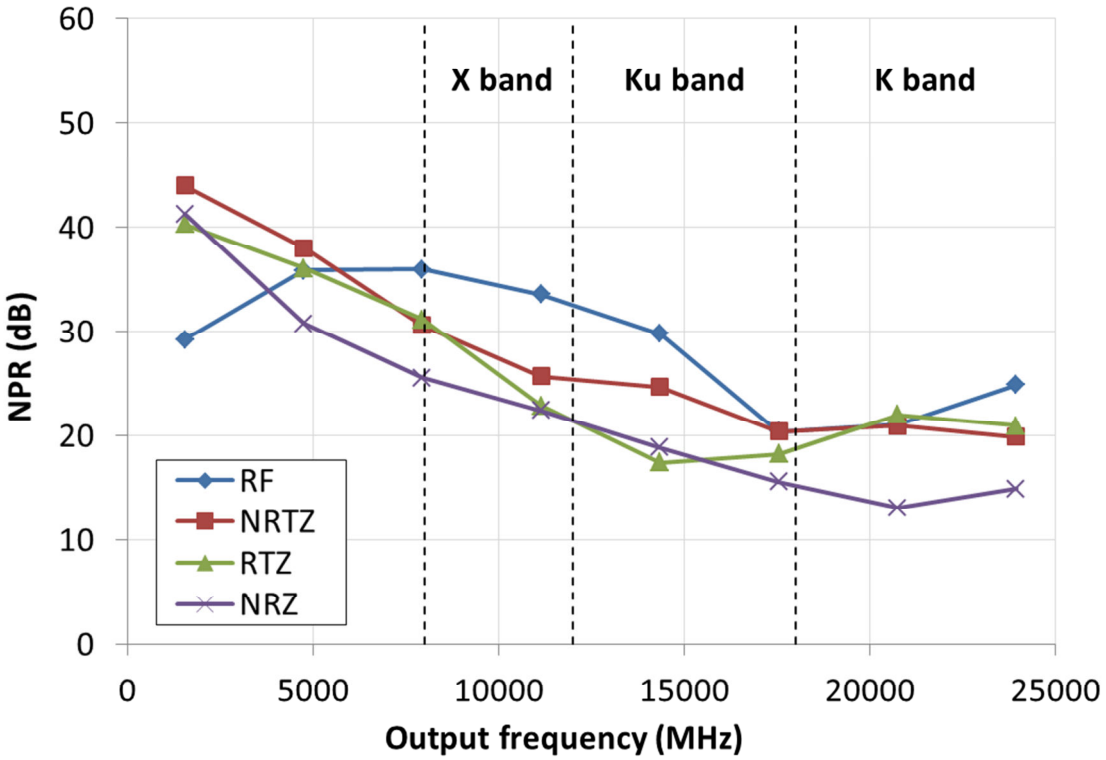
min: V_{CCA5}: 4.75V // V_{CCA3} = V_{CCD} = 3.15V
Typ: V_{CCA5}: 5.00V // V_{CCA3} = V_{CCD} = 3.30V
MAX: V_{CCA5}: 5.25V // V_{CCA3} = V_{CCD} = 3.45V





6.2.8.4 NPR over 8 Nyquist zones versus mode at 6.4 GSps

Figure 110. NPR vs Output Frequency from 1 GHz to 23 GHz, vs modes (covering X-Band, Ku-Band, K-Band)



6.2.8.5 NPR at 8.0 Gsps in IUCM2 and IUCM4 over Nyquist zones in RF mode

Figure 111. NPR vs Output Frequency at 8.0 Gsps in IUCM2 in RF mode over 6 Nyquist zones

NZ4 and NZ5 (2GHz width) are recommended to maximize output power together with NPR performance.

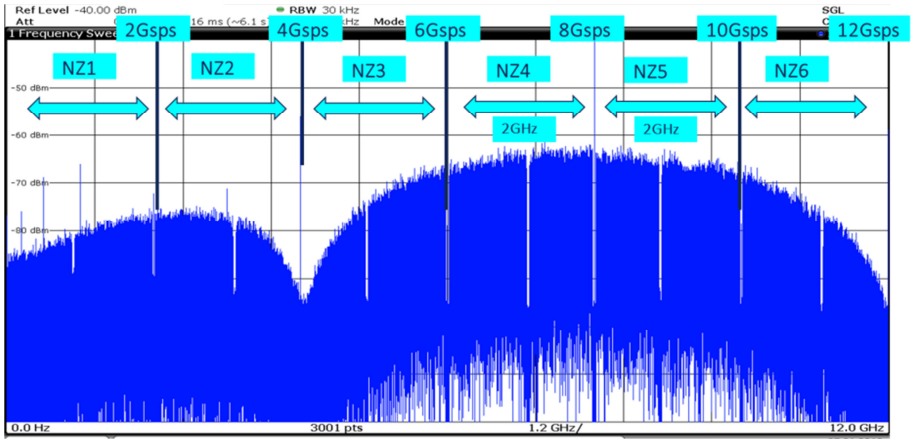


Figure 112. NPR vs Output Frequency at 8.0 Gsps in IUCM4 in RF mode over 12 Nyquist zones

NZ8 and NZ9 (1GHz width) are recommended to maximize output power together with NPR performance

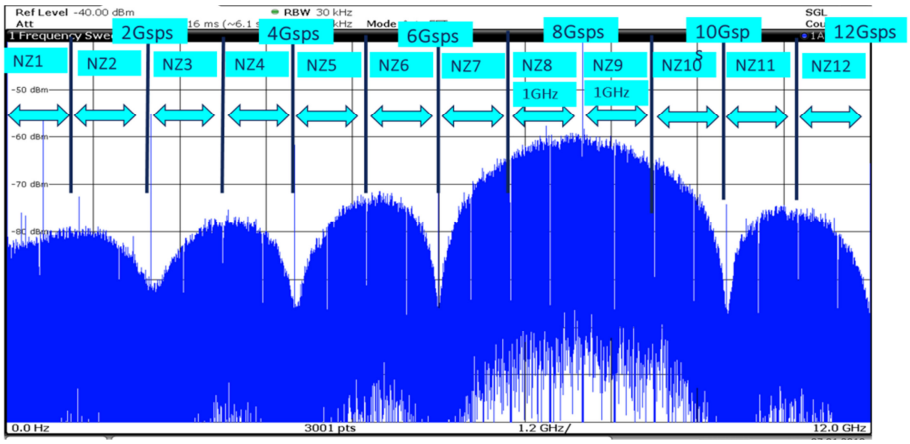


Figure 113. NPR vs Output Frequency at 8.0 Gsps in IUCM2 in RF mode in NZ4 (4th Nyquist zone)

NZ4 and NZ5 are recommended to maximize output power together with NPR performance in IUCM2 mode

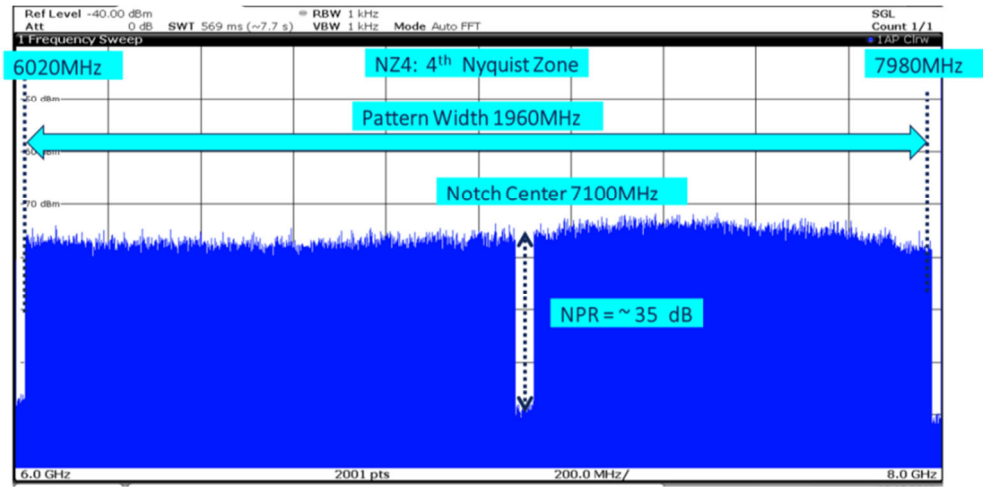


Figure 114. NPR vs Output Frequency at 8.0 Gsps in IUCM4 in RF mode in NZ8 (8th Nyquist zone)

NZ8 and NZ9 are recommended to maximize output power together with NPR performance in IUCM4 mode

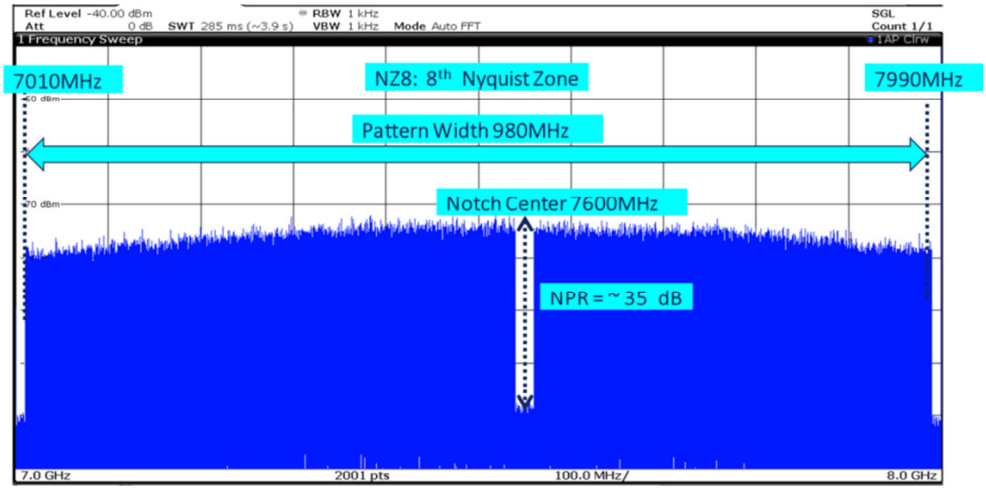


Figure 115. NPR at 8.0 Gsps in IUCM2 in RF mode in 4th Nyquist and 5th Nyquist Zone

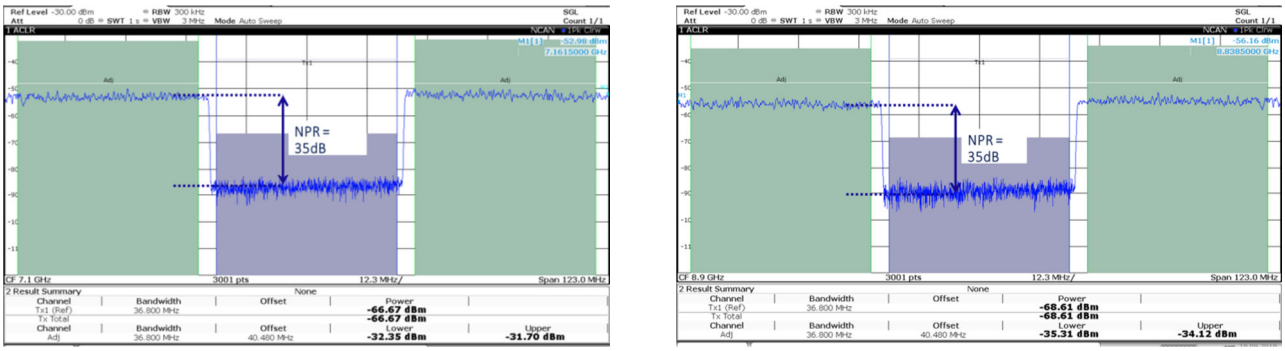
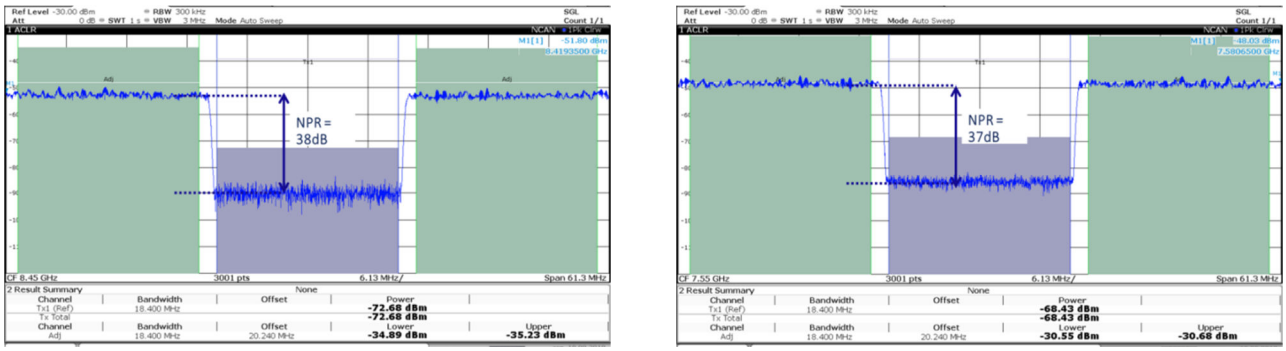


Figure 116. NPR at 8.0 Gsps in IUCM4 in RF mode in 8th Nyquist and 9th Nyquist Zone



6.2.8.6 NPR at 8.5 Gsps in IUCM2 and IUCM4 over Nyquist zones in RF mode

Figure 117. NPR vs Output Frequency at 8.5 Gsps in IUCM2 in RF mode over 12 Nyquist zones

NZ4 and NZ5 (2125MHz width) are recommended to maximize output power together with NPR performance.

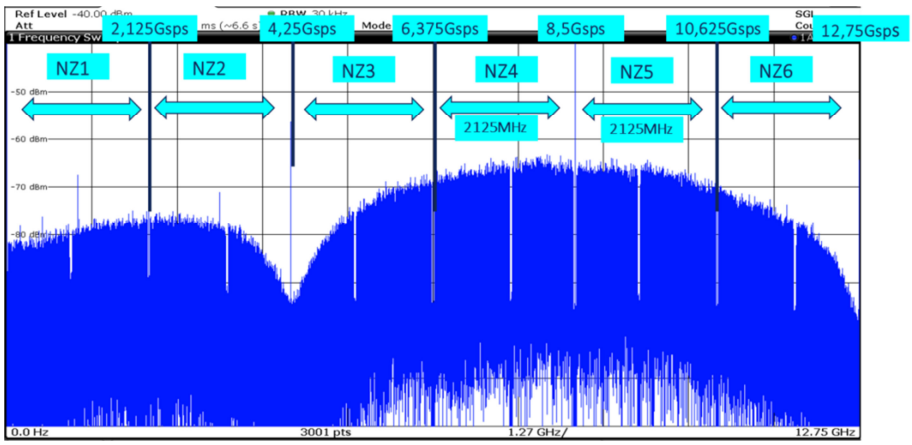


Figure 118. NPR vs Output Frequency at 8.5 Gsps in IUCM4 in RF mode over 6 Nyquist zones

NZ8 and NZ9 (1,0625 GHz width) are recommended to maximize output power together with NPR performance

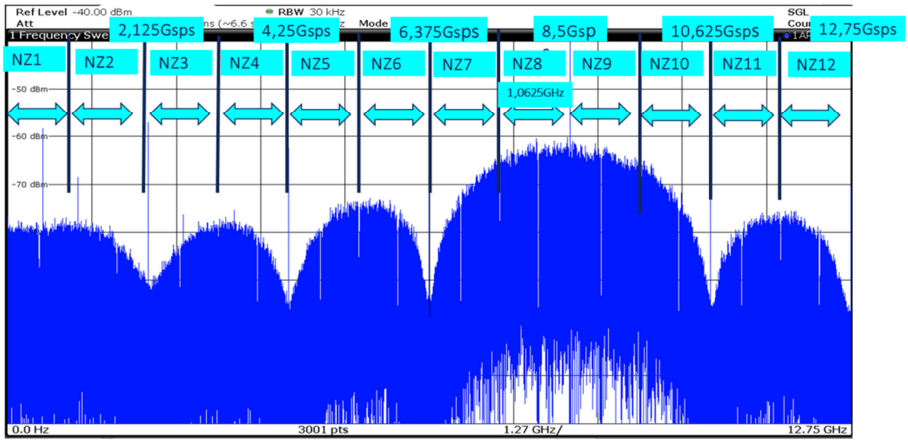


Figure 119. NPR at 8.5 Gsps in IUCM2 in RF mode in 4th Nyquist and 5th Nyquist Zone

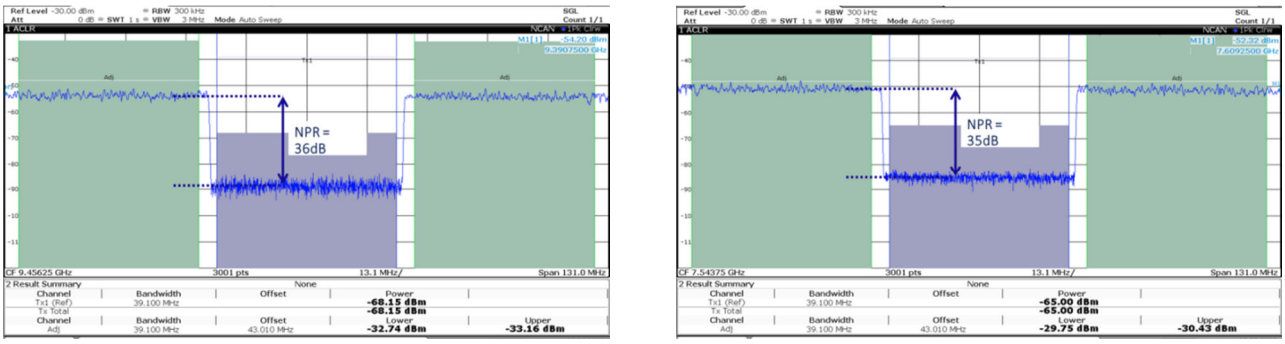
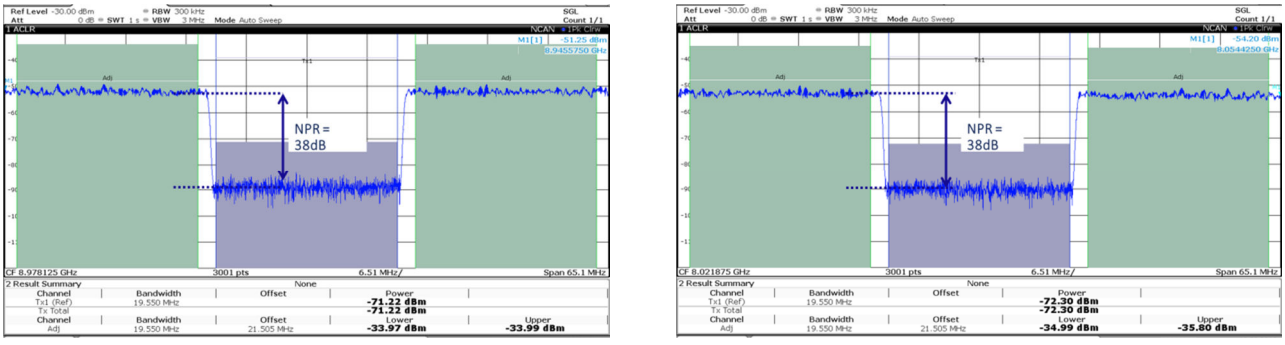


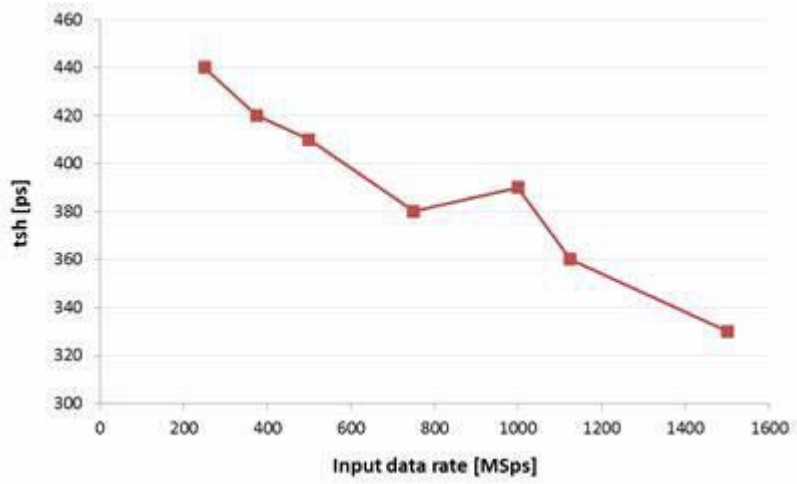
Figure 120. NPR at 8.5 Gsps in IUCM4 in RF mode in 8th Nyquist and 9th Nyquist Zone



6.3 Input Data Set-up and Hold time vs Input Data Rate

The figure below shows t_{SH} variation versus input data rate.

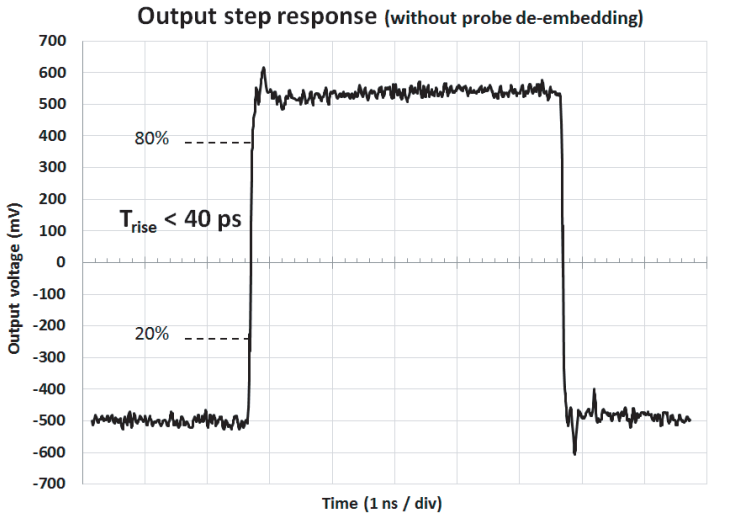
Figure 121. t_{SH} vs input data rate



6.4 Analog output rise and fall time

The figure below shows the DAC output step response with rise and fall time of 30 ps after probe de-embedding.

Figure 122. Analog output step response (Full Scale 1Vpp)



After the oscilloscope probe de-embedding, T_{rise} ≈ 30 ps → DAC bandwidth ≈ 7.5 GHz

7 APPLICATION INFORMATION

7.1 Analog output (OUT/OUTN)

The analog output should be used as a differential signal, as described in the figures below.

If the application requires a single-ended analog output, then a balun is necessary to generate a single ended signal from the differential output of the DAC.

Figure 123. Analog output differential termination

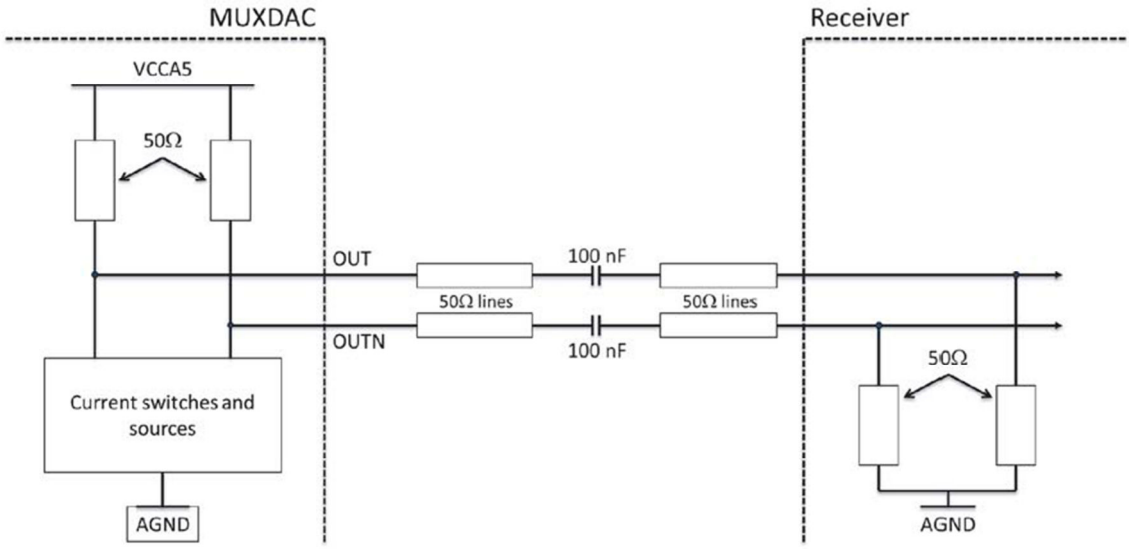
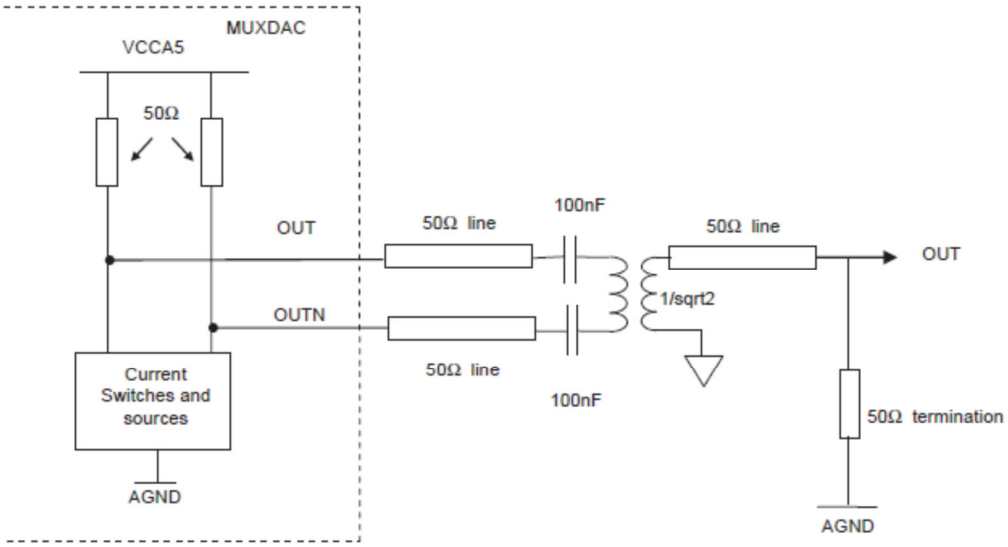


Figure 124. Analog output using a 1/sqrt(2) Balun



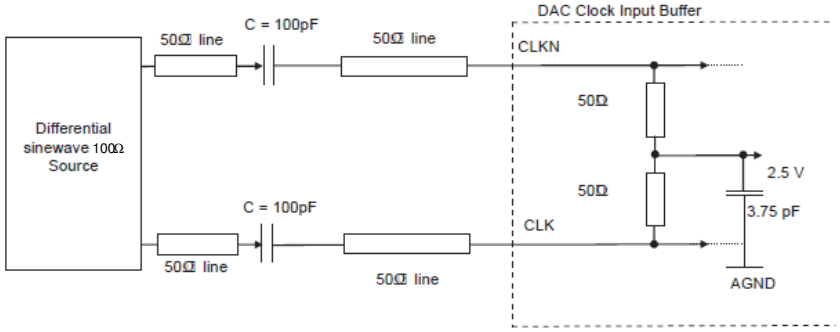
Note: The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application.

For proper high frequency operation up to the K-band, the outputs lines topology has to be carefully designed for optimum VSWR performances (See User Guide and Evaluation board).

7.2 Clock Input (CLK/CLKN)

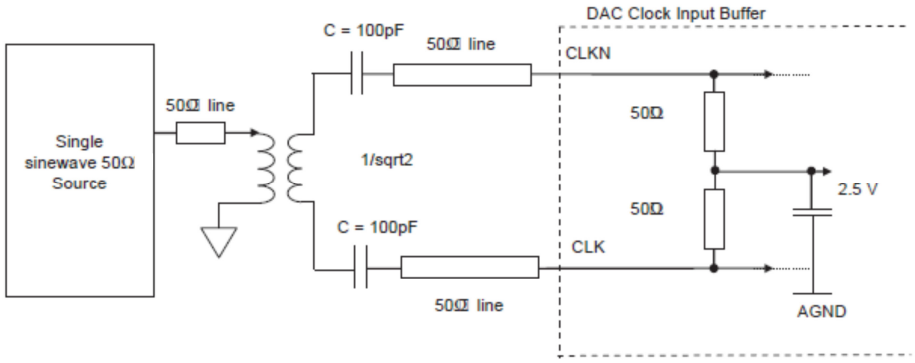
The DAC input clock (sampling clock) should be provided as a differential signal as described in the following figures:

Figure 125. Clock input differential termination



Note: The buffer is internally pre-polarized to 2.5V (buffer between V_{CCA5} and AGND).

Figure 126. Clock input differential with balun

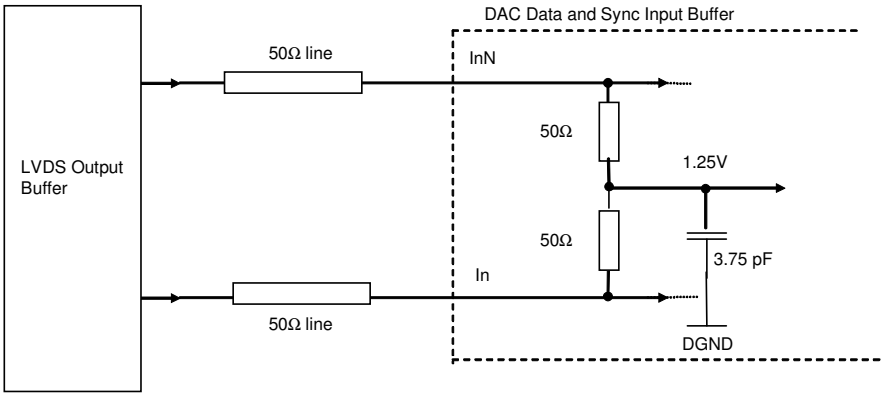


The AC coupling capacitors should be chosen as broadband capacitors with a value depending on the application).

7.3 Digital Data, SYNC and IDC inputs

LVDS buffers are used for the digital input data, the SYNC signal (active high) and the IDC signal. They are all internally terminated by 2 × 50Ω to ground via a 3.75 pF capacitor.

Figure 127. Digital data, SYNC and IDC input differential termination



Notes:

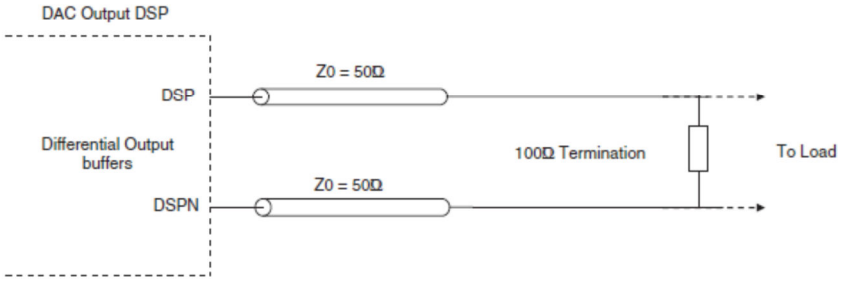
1. In the case when only two ports are used (2:1 MUX ratio), then the unused data can be left floating (unconnected).
2. Data and IDC signals should be routed on board with the same layout rules and the same length than the data
3. In case the SYNC is not used, it is recommended to bias the SYNC to 1.1V and SYNCN to 1.4V.

7.4 DSP Clock

The DSP, DSPN output clock signals are LVDS compatible.

If not used, they have to be terminated via a differential 100Ω termination as described in the following figure:

Figure 128. DSP output differential termination



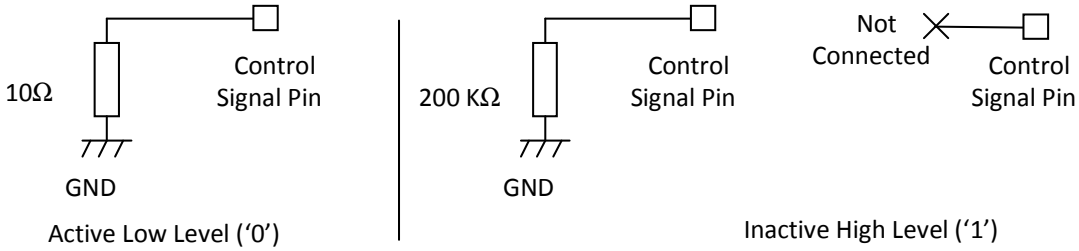
7.5 Control signal settings

The PSS and OCDS control signals use the same static input buffer.

Logic '1' = 200 KΩ to Ground, or tied to V_{CCD} = 3.3V or left open

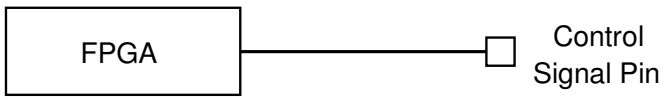
Logic '0' = 10Ω to Ground or Grounded

Figure 129. Control signal output differential termination



The control signals can be driven by an FPGA.

Figure 130. Control signal settings with FPGA



Logic 1 > VIH or V_{CCD} = 3.3V

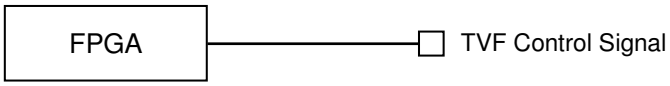
Logic 0 < VIL or 0V

7.6 TVF Control signal

The TVF control signal is a 3.3V CMOS output signal.

This signal could be acquired by FPGA.

Figure 131. Control signal settings with FPGA



In order to modify the VOL/VOH value, pull up and pull down resistor or a potential divider could be used.

7.7 Power Supply Decoupling and Bypassing

The DAC requires 3 distinct power supplies:

V_{CCA5} = 5.0V (for the analog core)

V_{CCA3} = 3.3V (for the analog part)

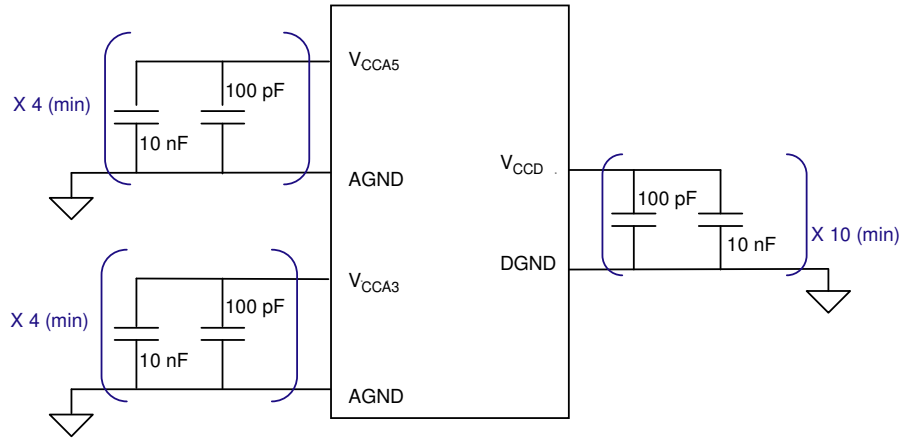
V_{CCD} = 3.3V (for the digital part)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 100 pF in parallel to 10nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighbouring pins.

4 pairs of 100pF in parallel to 10 nF capacitors are required for the decoupling of V_{CCA5}.

4 pairs for the V_{CCA3} and 10 pairs are necessary for V_{CCD}.

Figure 132. Power Supplies Decoupling Scheme



Each power supply has to be bypassed as close as possible to its source and accessed by 100 nF in parallel to 22 µF capacitors (the optimum value depends on the regulators).

7.8 Power on/off requirement and power on reset function

The DAC timing circuitry must be reset either by a power on reset (see below) or through the use of the SYNC input to set it to the right state. Refer to Section 5.10.

At power-up a reset pulse is internally and automatically generated when the following sequence is satisfied: V_{CCD}, V_{CCA3} then V_{CCA5}.

This pulse has two effects:

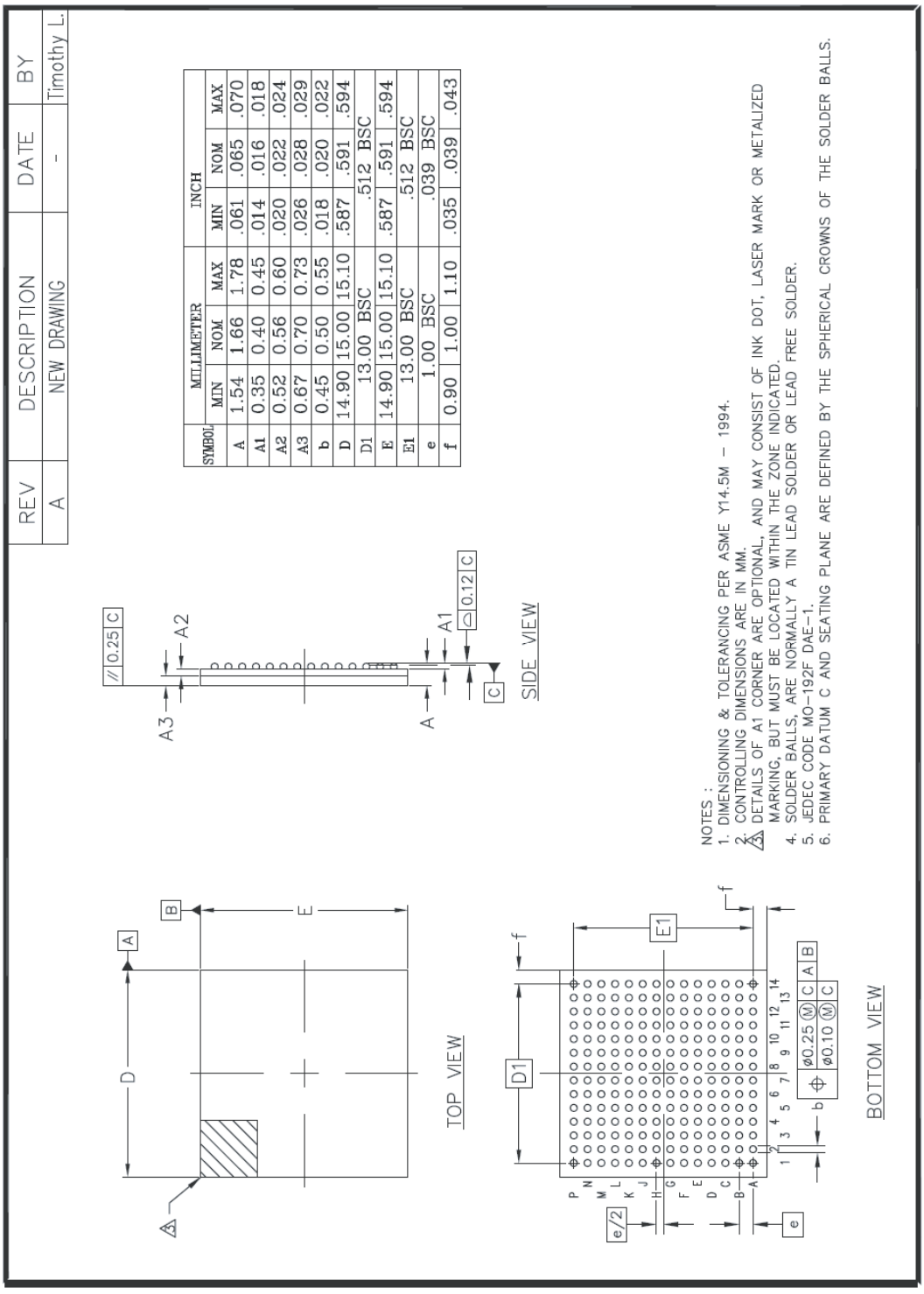
- Resetting of the 3WSI interface registers to their default values.
- Synchronizing the timing circuitry.

To cancel the SYNC pulse at power-up, it is necessary to apply the sequence: V_{CCA5} then V_{CCA3} and V_{CCD}. Any other sequence may not have a deterministic SYNC behaviour but can be used.

There is no specific requirement to power down the device.

8 PACKAGE DESCRIPTION

8.1 fpBGA 196 Outline



8.2 Thermal Characteristics

Assumptions:

- Still air
- Pure conduction
- No radiation
- Heating zone = 8.9% of die surface Rth Junction - bottom of Balls = 13°C/W

Rth Junction - board (JEDEC JESD-51-8) = 17.3°C/W Rth Junction - top of case = 14°C/W

Assumptions:

- Heating zone = 8.9% of die surface
- Still air, JEDEC condition

Rth Junction - ambient (JEDEC) = 32.0 °C/W

The hot spot point is 6°C above the temperature given by the diode

9 ORDERING INFORMATION

Table 27. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS480AZP	FpBGA196	Ambient	General Sample Prototype	
EVX12DS480AZPY	FpBGA196	Ambient	General Sample Prototype	
EV12DS480ACZPY	FpBGA196	0°C < Tc, Tj < 90°C	Commercial C Grade	
EV12DS480AMZP	FpBGA196	–55°C < Tc, Tj < 125°C	Military M Grade	
EV12DS480AMZP-E3	FpBGA196	–55°C < Tc, Tj < 125°C	ECSS Class 3	
EV12DS480AMZP-N1	FpBGA196	–55°C < Tc, Tj < 125°C	Nasa Level 1	
EV12DS4xxAZPY-EB	FpBGA196 RoHS	Ambient	Prototype	Evaluation Board

10 REVISION HISTORY

This table provides revision history for this document.

Table 28. Revision History

Rev. No	Date	Substantive Change(s)
DS 60S 217580(A.1)	February 2019	Initial Revision

Table of Contents

1 BLOCK DIAGRAM 2
2 DESCRIPTION 2
3 ELECTRICAL CHARACTERISTICS 3
3.1 Absolute Maximum ratings 3
3.2 Recommended conditions of use 4
3.3 DC Electrical Characteristics 5
3.4 AC Electrical Characteristics 7
3.5 Timing Characteristics and Switching Performance 16
3.6 Explanation of Test Levels 20
3.7 Digital Input Coding Table 20
4 DEFINITION OF TERMS 21
5 FUNCTIONAL DESCRIPTION 22
5.1 Multiplexer 23
5.2 Mode Function 23
5.2.1 NRZ output mode 25
5.2.2 Narrow RTZ (NRTZ) output mode 25
5.2.3 RTZ output Mode 26
5.2.4 RF output mode 26
5.3 RPW and RPB Feature 27
5.4 Phase Shift Select function (PSS) 30
5.5 Output Clock Division Select function (OCDS) 32
5.6 Input Under Clocking Mode (IUCM) 32
5.7 Multiplexer Delay Adjust (MDA) 35
5.8 Synchronization FPGA-DAC: IDC_P, IDC_N and TVF function 35
5.9 DSP output clock 36
5.10 OCDS, IUCM and MUX combinations summary 37
5.11 Synchronization function 37
5.12 Gain Adjust function 37
5.13 Diode function 38
5.14 DAC 3WSI Description (DAC Controls) 38
5.14.1 3WSI timing description 38
5.14.2 3WSI: Address and Data Description 39
5.14.3 State Register (address 0000) 40
5.14.4 GA Register (address 0001) 42
5.14.5 DSP Register (address 0101) 42
6. PIN DESCRIPTION 43
6 CHARACTERIZATION RESULTS 48
6.1 Static performance 48
6.1.1 INL/DNL 48
6.1.2 DC Gain 48
6.2 AC performance 49
6.2.1 Available Output Power vs Fout. 49
6.2.2 Single Tone SFDR Measurements versus Fout 54
6.2.3 Single Tone Spectrum versus Fout and Output Modes 55
6.2.4 Single Tone SFDR Measurements versus Fclock (MUX 4:1) 66

6.2.5 SFDR vs Power supplies & Temperature 66
6.2.6 Dual Tones Spectra 67
6.2.7 ACPR measurements @ 6.0 GSps (10 MHz QPSK) 72
6.2.8 NPR performance 75
6.3 Input Data Set-up and Hold time vs Input Data Rate 83
6.4 Analog output rise and fall time 83
7 APPLICATION INFORMATION 84
7.1 Analog output (OUT/OUTN) 84
7.2 Clock Input (CLK/CLKN) 85
7.3 Digital Data, SYNC and IDC inputs 85
7.4 DSP Clock 86
7.5 Control signal settings 86
7.6 TVF Control signal 86
7.7 Power Supply Decoupling and Bypassing 87
7.8 Power on/off requirement and power on reset function 87
8 PACKAGE DESCRIPTION 88
8.1 fpBGA 196 Outline 88
8.2 Thermal Characteristics 89
9 ORDERING INFORMATION 89
10 REVISION HISTORY 89

Table of Figures

Figure 1. Simplified block diagram 2
Figure 2. Timing Diagram for 4:1 MUX principle of operation OCDS1, IUCM1 17
Figure 3. Timing diagram for 4:1 MUX principle of operation, IUCM2 18
Figure 4. Timing Diagram for 4:1 MUX principle of operation OCDS1, IUCM4 18
Figure 5. Timing Diagram for 2:1 MUX principle of operation OCDS1, IUCM1 18
Figure 6. Timing relationship between SYNC and DSP 18
Figure 7. SYNC Timing Diagram 19
Figure 8. DAC functional diagram 22
Figure 9. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 6.4 GSps in IUCM1, over four Nyquist zones, computed for different RPW steps 24
Figure 10. Max available output power (Pout) at nominal gain vs output frequency (Fout) in the four output modes at 3.2 GSps, over eight Nyquist zones, computed for different RPW steps 25
Figure 11. NRZ timing diagram 25
Figure 12. Narrow RTZ timing diagram 26
Figure 13. RTZ timing diagram 26
Figure 14. RF timing diagram 27
Figure 15. DAC output in NRZ and time domain 27
Figure 16. DAC output in RTZ mode and time domain when RPB is optimum 28
Figure 17. DAC output in RTZ mode and time domain when RPB is not optimum 28
Figure 18. DAC output in NRTZ mode and time domain when RPB/RPW are optimum 29
Figure 19. DAC output in NRTZ mode and time domain when RPB is not optimum 29
Figure 20. DAC output in NRTZ mode and time domain when RPW is not optimum 29
Figure 21. DAC output in RF mode and time domain when RPB and RPW are optimum 30
Figure 22. PSS timing diagram for 4:1 MUX, OCDS = 0 31
Figure 23. PSS timing diagram for 2:1 MUX, OCDS = 0 31
Figure 24. OCDS timing diagram for 4:1 MUX and IUCM1 mode 32
Figure 25. OCDS timing diagram for 2:1 MUX and IUCM1 mode 32
Figure 26. Pout curves in RF mode at 8.0 GSps from DC to 12 GHz in IUCM1, IUCM2 and IUCM4 modes 33
Figure 27. Pout curves at 8.0 GSps from DC to 12 GHz in IUCM1,IUCM2 and IUCM4 modes (Zoom around 8GHz) 33
Figure 28 Max available Pout at nominal gain vs Fout in the four output modes at 8.0 GSps, combined with IUCM4, over 16 Nyquist zones, computed for different RPW steps 34
Figure 29. Max available Pout at nominal gain vs Fout in the four output modes at 8.0 GSps, combined with IUCM2, over 16 Nyquist zones, computed for different RPW steps 35
Figure 30. IDC timing vs data input 35
Figure 31. FPGA to DAC synoptic 36
Figure 32. Temperature diode implementation 38
Figure 33. Diode Characteristics for Die Junction Temperature Monitoring 38
Figure 34. 3WSI Timing Diagram 39
Figure 35. Pinout view fpBGA196 (Top view) 43
Figure 36. INL & DNL measurements at Fout = 100 kHz, Fclock = 3 GHz 48
Figure 37. Output Voltage variations versus Gain Adjust 48
Figure 38. Output voltage variation vs Power supplies & temperature vs Gain Adjust 48
Figure 39. Pout vs Fout from 32 MHz to 4768 MHz in the 4 output modes at 3.2 GSps in MUX2:1 49
Figure 40. Pout vs Fout @ 6.4 GSps from DC to 9 GHz vs modes 49
Figure 41. Pout vs Fout @ 6.4 GSps from 8 GHz to 26 GHz vs modes (includes X-Band, Ku-Band and K Band) 50
Figure 42. Pout vs Fout @ 6.4 GSps from 8 GHz to 12 GHz vs modes (X-Band) 50
Figure 43. Pout vs Fout @ 6.4 GSps from 12 GHz to 18 GHz vs modes (Ku-Band) 50
Figure 44. Pout vs Fout @ 6.4 GSps from 12 GHz to 26 GHz vs modes (K-Band) 51
Figure 45. Pout vs Fout @ 8.0 GSps from DC to 26 GHz, IUCM1, IUCM2 and IUCM4 in RF mode 51
Figure 46. Pout vs Fout @ 8.0 GSps from 5GHz to 11 GHz , IUCM1, IUCM2 and IUCM4 in RF mode 52
Figure 47. Pout vs Fout @ 8.5 GSps from DC to 26 GHz , IUCM1, IUCM2 and IUCM4 in RF mode 52
Figure 48. Pout vs Fout @ 8.5 GSps from 5.3125 GHz to 11.6875 GHz , IUCM1, IUCM2 and IUCM4 in RF mode 53
Figure 49. SFDR in the 4 output modes at 6.4 GSps in MUX4:1 54
Figure 50. SFDR in the 4 output modes at 3.2 GSps in MUX2:1 54
Figure 51. SFDR (dBc) vs Fout from 5 GHz to 35 GHz (covering X-Band, Ku-Band, K-Band and Ka-Band) @ 6.4 GSps in MUX4:1, RF mode 55
Figure 52. Typical SFDR spectrum in NRTZ mode with Fout = 3136 MHz (1st Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 60 dBc 55
Figure 53. Typical SFDR spectrum in NRTZ mode with Fout = 6336 MHz (2nd Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 53 dBc 56
Figure 54. Typical SFDR spectrum in RF mode with Fout = 9536 MHz (3rd Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 50 dBc 56
Figure 55. Typical SFDR spectrum in RF mode with Fout = 12736 MHz (4th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 47 dBc 57
Figure 56. Typical SFDR spectrum in NRTZ mode with Fout = 15936 MHz (5th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR

= 37 dBc 57
Figure 57. Typical SFDR spectrum in RF mode with Fout = 19146 MHz (6th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 40 dBc 57
Figure 58 Typical SFDR spectrum in RF mode with Fout = 22336 MHz (7th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 34 dBc 58
Figure 59 Typical SFDR spectrum in RF mode with Fout = 25536 MHz (8th Nyquist), MUX4:1, Fs = 6.4 GSps, SFDR = 44 dBc 58
Figure 60. Typical SFDR spectrum in NRTZ mode with Fout = 3430 MHz (1st Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 55 dBc 59
Figure 61. Typical SFDR spectrum in RF mode with Fout = 6930 MHz (2nd Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 58 dBc 59
Figure 62. Typical SFDR spectrum in RF mode with Fout = 10430 MHz (3rd Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 50 dBc 60
Figure 63. Typical SFDR spectrum in RF mode with Fout = 13930 MHz (4th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 48 dBc 61
Figure 64. Typical SFDR spectrum in RF mode with Fout = 17430 MHz (5th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 41 dBc 61
Figure 65. Typical SFDR spectrum in RF mode with Fout = 20930 MHz (6th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 36 dBc 61
Figure 66. Typical SFDR spectrum in RF mode with Fout = 24430 MHz (7th Nyquist), MUX4:1, Fs = 7.0 GSps, SFDR = 37 dBc 62
Figure 67. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ4 (Fout = 6040MHz) and (Fout=7960MHz), Fs = 8.0 GSps 62
Figure 68. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ5 (Fout = 8040 MHz) and Fout = 9960 MHz, Fs = 8.0 GSps 62
Figure 69. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ8 (Fout = 7020 MHz) and (Fout = 7980 MHz), Fs = 8.0 GSps 63
Figure 70. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ9 (Fout = 8020 MHz) and (Fout = 8980MHz), Fs = 8.0 GSps 63
Figure 71. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ4 (Fout = 6417 MHz) and (Fout = 7960 MHz), Fs = 8.5 GSps 63
Figure 72. Typical SFDR spectrum in RF mode in IUCM2 Mode in NZ5 (Fout = 8542 MHz) and (Fout = 10582 MHz), Fs = 8.5 GSps 64
Figure 73. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ8 (Fout = 7458 MHz) and (Fout = 8478 MHz), Fs = 8.5 GSps 64
Figure 74. Typical SFDR spectrum in RF mode in IUCM4 Mode in NZ9 (Fout = 8521 MHz) and (Fout = 9541 MHz), Fs = 8.5 GSps 64
Figure 75. Typical SFDR spectrum in NRZ mode. Fout = 32 MHz (1st Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 70 dBc 65
Figure 76. Typical SFDR spectrum in NRTZ mode. Fout = 32 MHz (1st Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 76 dBc 65
Figure 77.Typical SFDR spectrum in NRTZ mode. Fout = 1568 MHz (1st Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 65 dBc 65
Figure 78. Typical SFDR spectrum in RTZ mode. Fout = 3168 MHz (2nd Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 59 dBc 65
Figure 79. Typical SFDR spectrum in RF mode. Fout = 3168 MHz (2nd Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 58 dBc 65
Figure 80. Typical SFDR spectrum in RF mode. Fout = 4768 MHz (3rd Nyquist), MUX2:1, Fs = 3.2 GSps. SFDR = 53 dBc 65
Figure 81. SFDR versus Fclk in 1st Nyquist zone for 4 output modes. Fout = Fclk/2 - Fclk/100 66
Figure 82. SFDR versus Fclk in 2nd Nyquist zone for 3 output modes. Fout = Fclk - Fclk/100 66
Figure 83. SFDR vs Power supplies vs modes 66
Figure 84. SFDR vs temperature vs modes 66
Figure 85. Typical Dual-tone IMD3- to IMD9- (highest spur) versus (Fout1, Fout2) from 6000 MHz to 23000MHz, Fs = 6.4 GSps, (Fout1-Fout2 =10MHz apart) in RF mode 67
Figure 86. Typical Dual-tone spectrum in NRTZ mode with Fout1,Fout2 = 2950 MHz,2960 MHz (1st Nyquist), MUX4:1, Fs = 6.4 GSps, IMD3 - = 70 dBc, IMD full Nyquist = 50 dBc 67
Figure 87. Typical Dual-tone spectrum in RF mode with Fout1, Fout2 = 6150 MHz,6160 MHz, (2nd Nyquist), MUX4:1, Fs = 6.4 GSps, IMD7 - = 67 dBc, IMD full Nyquist = 44 dBc 69
Figure 88. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 9150 MHz,9160 MHz (3rd Nyquist), MUX4:1, Fs = 6.4 GSps, IMD5 - = 55 dBc, IMD full Nyquist = 44 dBc 69
Figure 89. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 12550 MHz,12560 MHz (4th Nyquist), MUX4:1, Fs = 6.4 GSps, IMD3 - = 56 dBc, IMD full Nyquist = 38 dBc 69
Figure 90. Typical Dual-tone spectrum in NRTZ mode with Fout1,Fout2 = 3450 MHz, 3460 MHz (1st Nyquist), MUX4:1,

Fs = 7.0 GSps, IMD3 - = 53 dBc, IMD full Nyquist = 51 dBc 70
Figure 91. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 6950 MHz,6960 MHz (2nd Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 64 dBc, IMD full Nyquist = 59 dBc 70
Figure 92. Typical Dual-tone spectrum in RF mode with Fout1,Fout2 = 10450 MHz,10460 MHz (3rd Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 52 dBc, IMD full Nyquist = 44 dBc 71
Figure 93. Typical Dual-tone spectrum in NRTZ mode with Fout1,Fout2 = 13950 MHz,13960 MHz, (4th Nyquist), MUX4:1, Fs = 7.0 GSps, IMD3 - = 54 dBc, IMD full Nyquist = 48 dBc..... 71
Figure 94. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 1.6 GHz Center frequency, ACPR = 59 dBc, NRTZ mode 72
Figure 95. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 4.6 GHz Center frequency, ACPR = 52 dBc, NRTZ mode 72
Figure 96. Adjacent Channel Power Ratio (ACPR)@ 6.0 GSps, 10 MHz QPSK, 10.6 GHz Center frequency, ACPR = 42 dBc, RF mode..... 73
Figure 97. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 16.6 GHz Center frequency, ACPR = 36.7 dBc, RF mode..... 73
Figure 98. Adjacent Channel Power Ratio (ACPR) @ 6.0 GSps, 10 MHz QPSK, 22.6 GHz Center frequency, ACPR = 30 dBc, RF mode..... 73
Figure 99. Adjacent Channel Power Ratio (ACPR) @ 7.0 GSps, 10 MHz QPSK, 22.9 GHz Center frequency, ACPR = 35 dBc, RF mode..... 74
Figure 100. NPR versus Loading Factor @ 6.4 Gsps (optimum NPR value is achieved for LF = –14 dBFS) 75
Figure 101. NPR in 1st Nyquist Zone, NRTZ mode, DC to 3200MHz, 90% Nyquist = 2880MHz Noise Pattern with a 60 MHz Notch Centered on 1440 MHz 75
Figure 102. NPR in 2nd Nyquist Zone, 3200 MHz to 6400 MHz with 90% Noise Pattern with a 60 MHz Notch Centered on 4960 MHz, NRTZ mode. 76
Figure 103. NPR in 2nd Nyquist Zone, 3200 MHz to 6400 MHz with 90% Noise Pattern with a 60 MHz Notch Centered on 4960 MHz, RF mode. 76
Figure 104. NPR in 3rd Nyquist Zone, 6400 MHz to 9600 MHz with 90% Noise Pattern with a 60 MHz Notch Centered on 7840 MHz, RF mode. 76
Figure 105. NPR @ 7.0 GSps in 1st Nyquist, 3150 MHz pattern, NPR = 42.6 dB (= 8.6 Bit ENOB), NRTZ mode..... 77
Figure 106. NPR @ 7.0 GSps in 2nd Nyquist, 3150 MHz pattern, NPR = 36.2 dB (= 7.6 Bit ENOB), NRTZ mode 77
Figure 107. NPR @ 7.0 GSps in 3rd Nyquist, 3150 MHz pattern, NPR = 33.3 dB (= 7.1 Bit ENOB), RF mode..... 77
Figure 108. NPR vs power supply in the 4 output modes at room temperature 78
Figure 109. NPR versus temperature at 6.0 GSps For the 4 output modes from Tc = –55°C to Tc = 95°C (Tj = –21°C to 125°C) 78
Figure 110. NPR vs Output Frequency from 1 GHz to 23 GHz, vs modes (covering X-Band, Ku-Band, K-Band) 78
Figure 111. NPR vs Output Frequency at 8.0 Gsps in IUCM2 in RF mode over 6 Nyquist zones 79
Figure 112. NPR vs Output Frequency at 8.0 Gsps in IUCM4 in RF mode over 12 Nyquist zones 79
Figure 113. NPR vs Output Frequency at 8.0 Gsps in IUCM2 in RF mode in NZ4 (4th Nyquist zone) 80
Figure 114. NPR vs Output Frequency at 8.0 Gsps in IUCM4 in RF mode in NZ8 (8th Nyquist zone) 80
Figure 115. NPR at 8.0 Gsps in IUCM2 in RF mode in 4th Nyquist and 5th Nyquist Zone 81
Figure 116. NPR at 8.0 Gsps in IUCM4 in RF mode in 8th Nyquist and 9th Nyquist Zone 81
Figure 117. NPR vs Output Frequency at 8.5 Gsps in IUCM2 in RF mode over 12 Nyquist zones 81
Figure 118. NPR vs Output Frequency at 8.5 Gsps in IUCM4 in RF mode over 6 Nyquist zones 82
Figure 119. NPR at 8.5 Gsps in IUCM2 in RF mode in 4th Nyquist and 5th Nyquist Zone 82
Figure 120. NPR at 8.5 Gsps in IUCM4 in RF mode in 8th Nyquist and 9th Nyquist Zone 82
Figure 121. t_{SH} vs input data rate 83
Figure 122. Analog output step response (Full Scale 1Vpp)..... 83
Figure 123. Analog output differential termination 84
Figure 124. Analog output using a 1/sqrt(2) Balun 84
Figure 125. Clock input differential termination 85
Figure 126. Clock input differential with balun 85
Figure 127. Digital data, SYNC and IDC input differential termination 85
Figure 128. DSP output differential termination 86
Figure 129. Control signal output differential termination 86
Figure 130. Control signal settings with FPGA 86
Figure 131. Control signal settings with FPGA 86
Figure 132. Power Supplies Decoupling Scheme 87