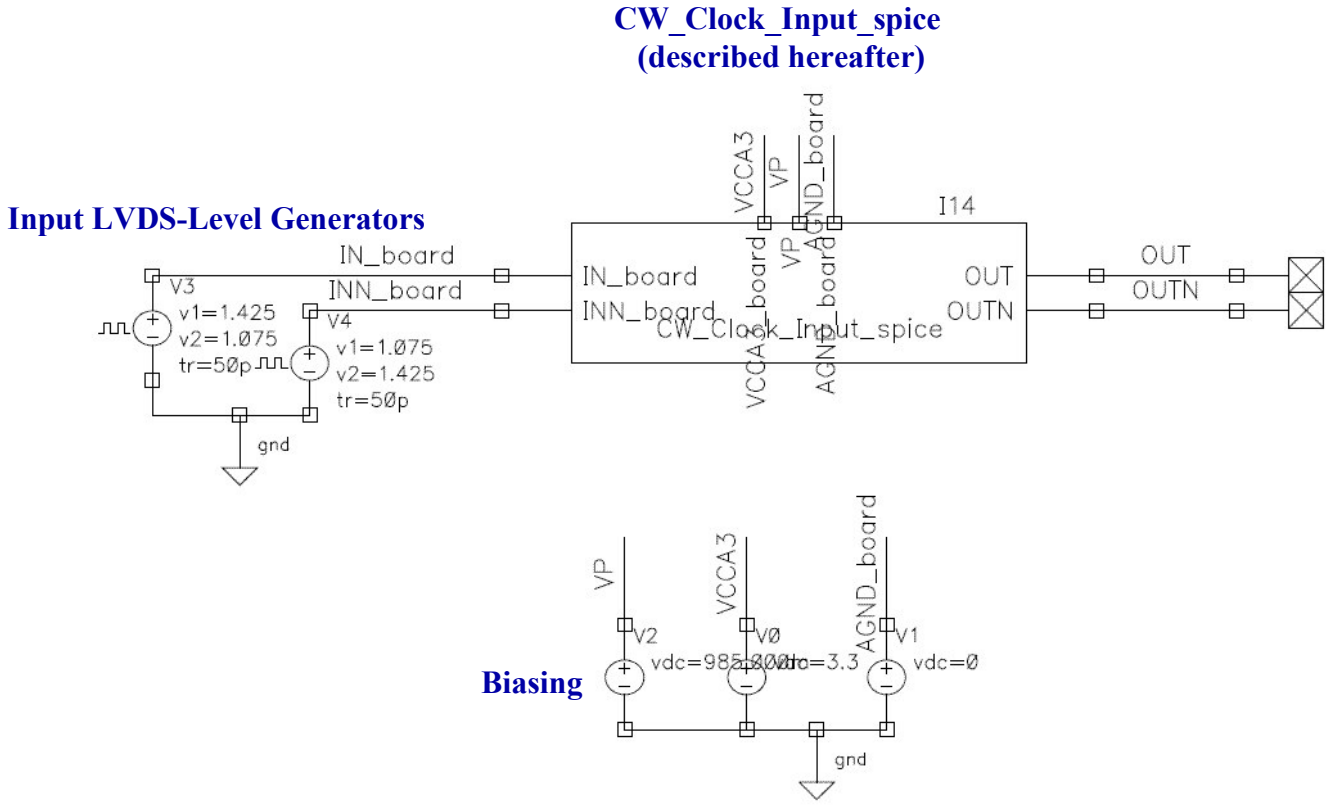
EV12DS130

Spice Models

CW Clock Input Buffer (transient + VSWR)

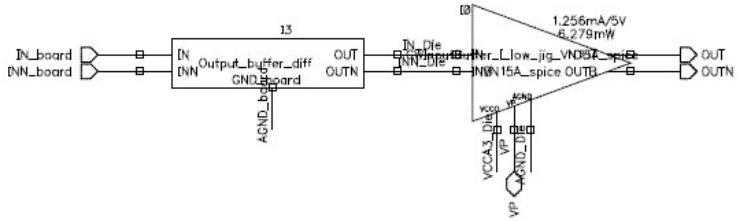
June 4th 2010

Top Level Simulation Schematic (Transient)

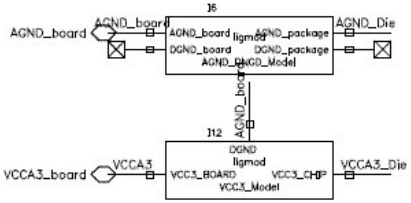


TOP CW Clock Input Schematic

Output_buffer_diff **CW_Input_Buffer_I_low_jig_VN15A_spice**



AGND_DGND_Model



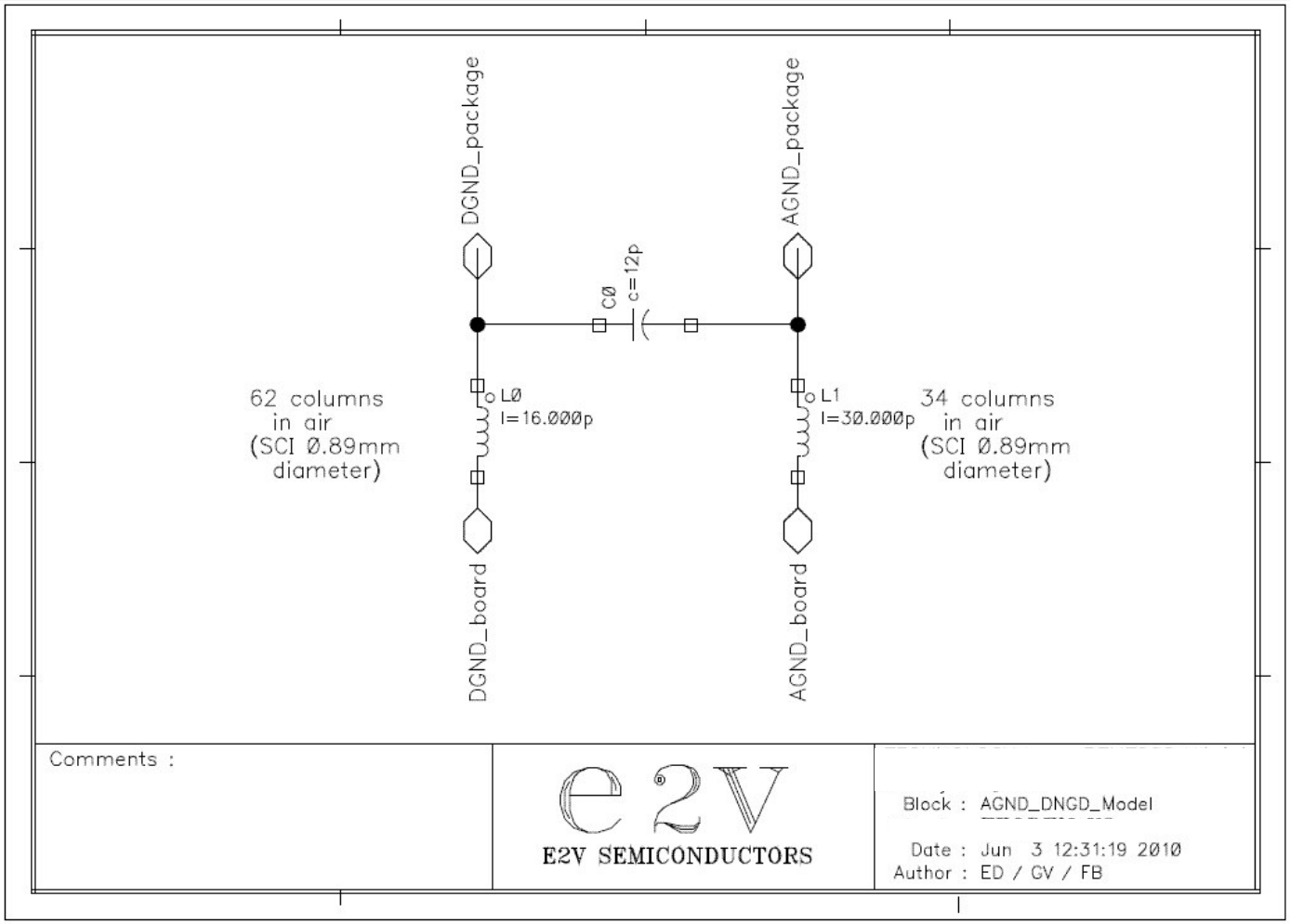
VCC3_Model

Comments :
Clock Input Buffer with
– Differential Input Transmission Lines
– Power Supply and Ground Package Models

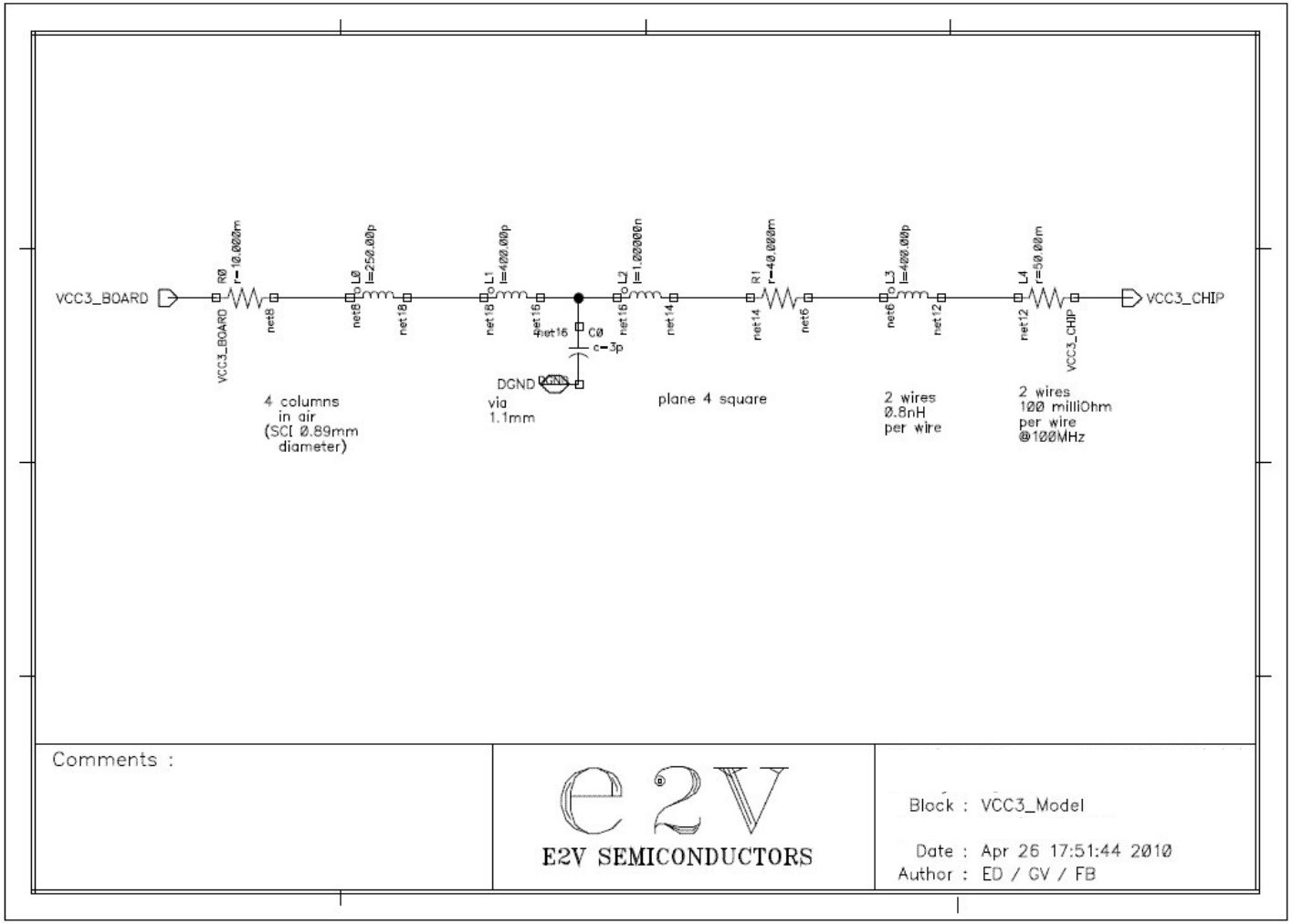
E2V SEMICONDUCTORS

Block : CW_Clock_Input_spice
Date : Jun 3 12:21:08 2010
Author : ED / GV / FB

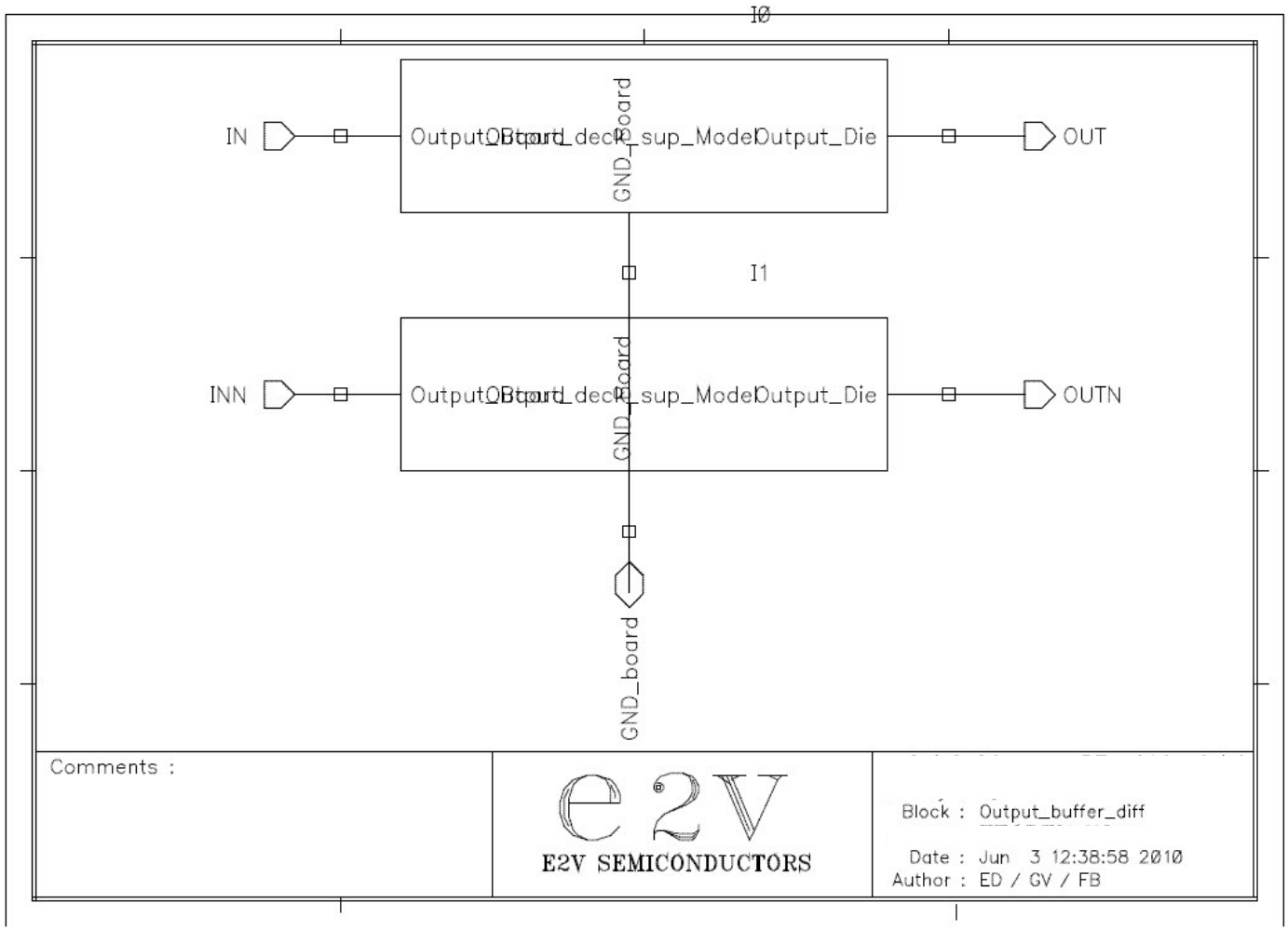
Ground Package Model
AGND & DGND



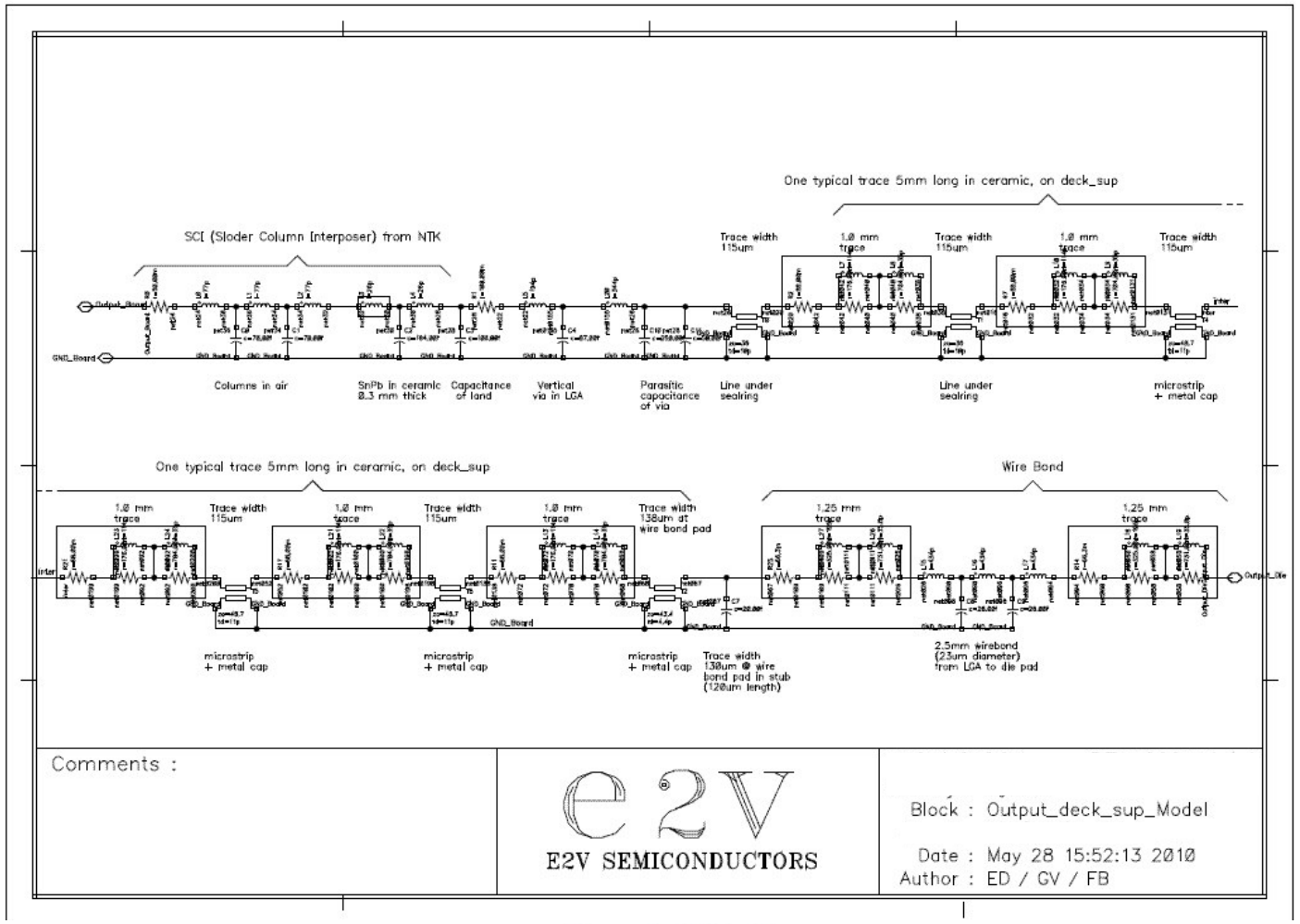
Power Supply Package Model
VCCA3



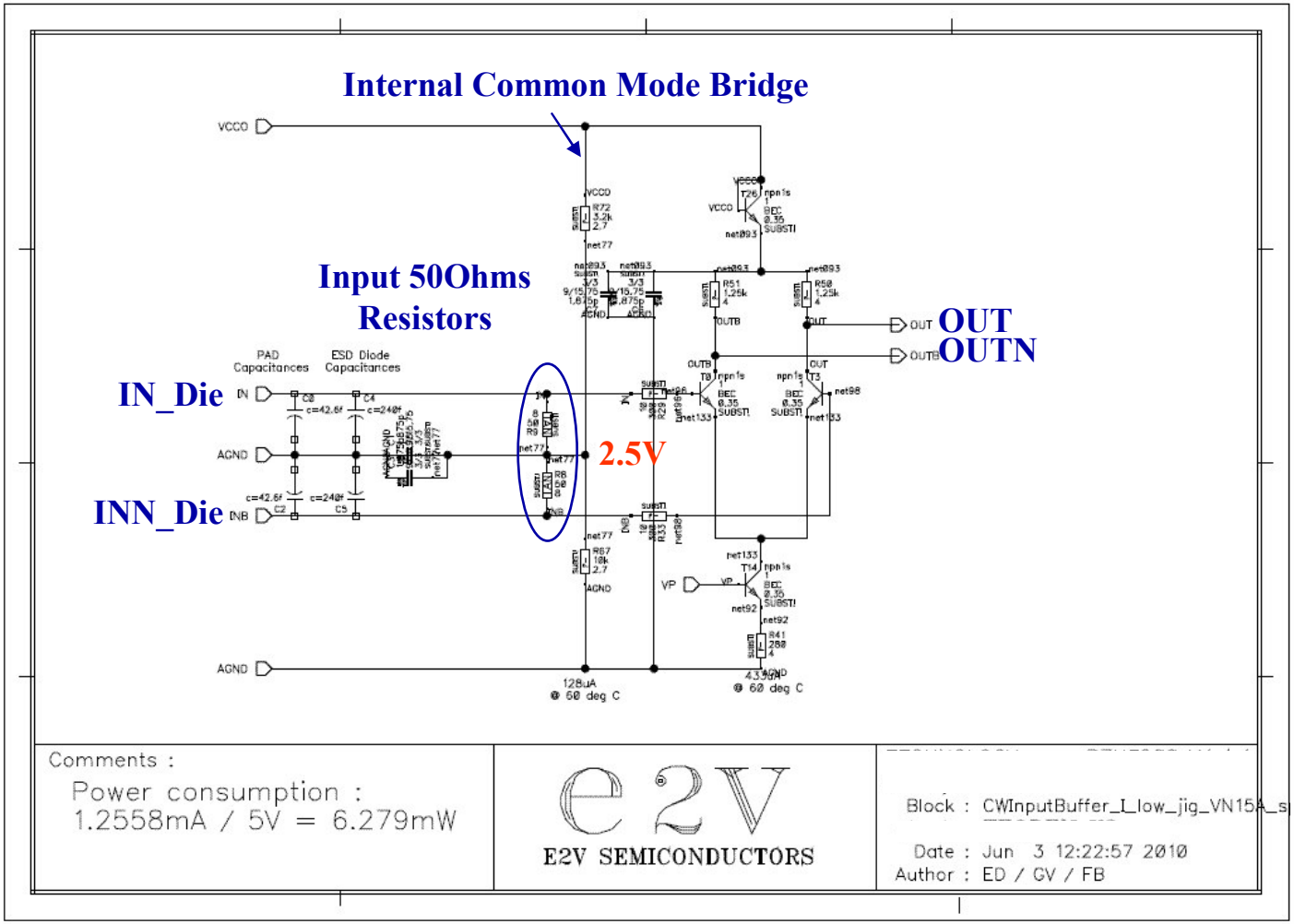
I/O Lines Package Models in Differential



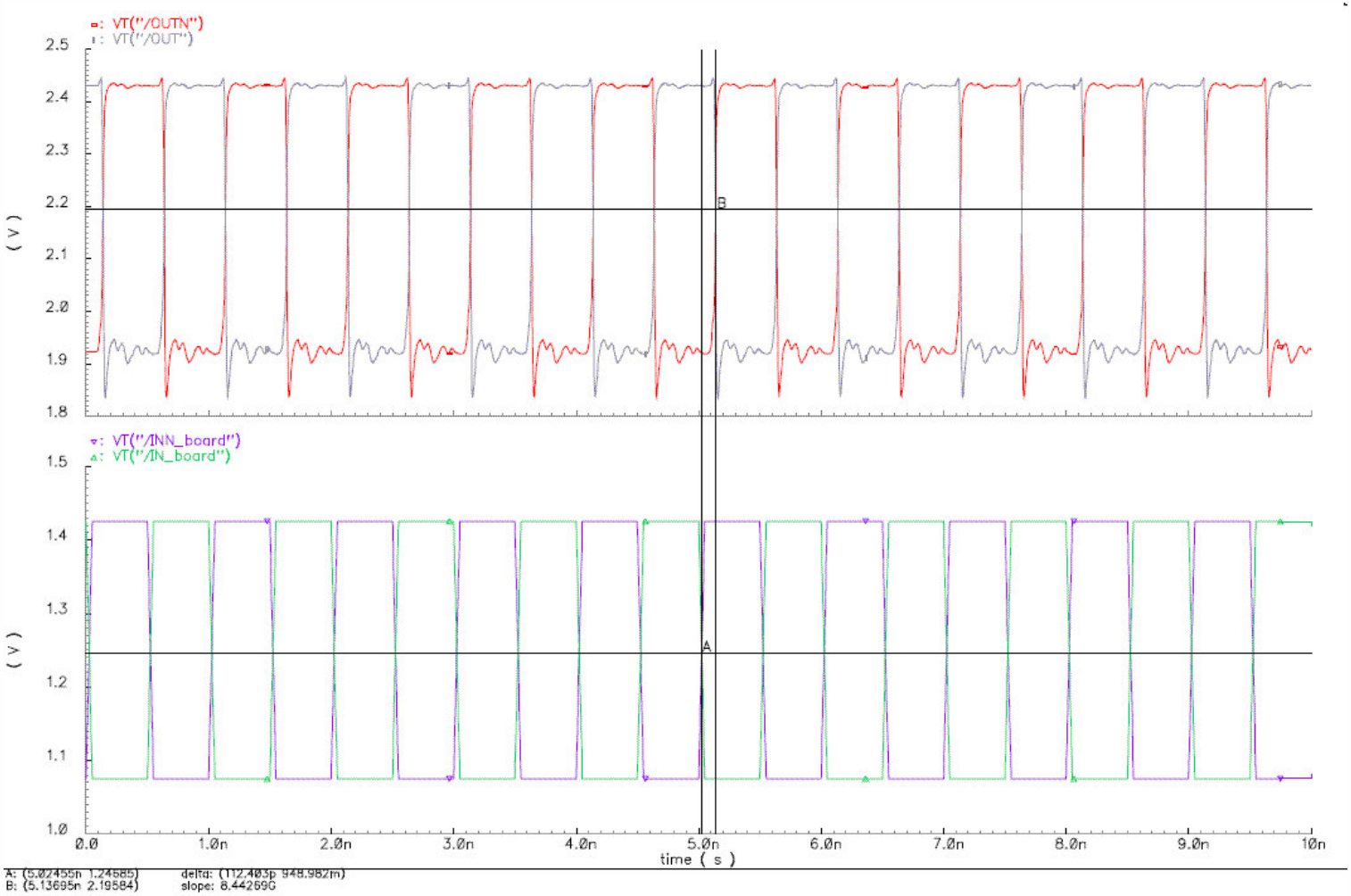
I/O Lines Package Model Single



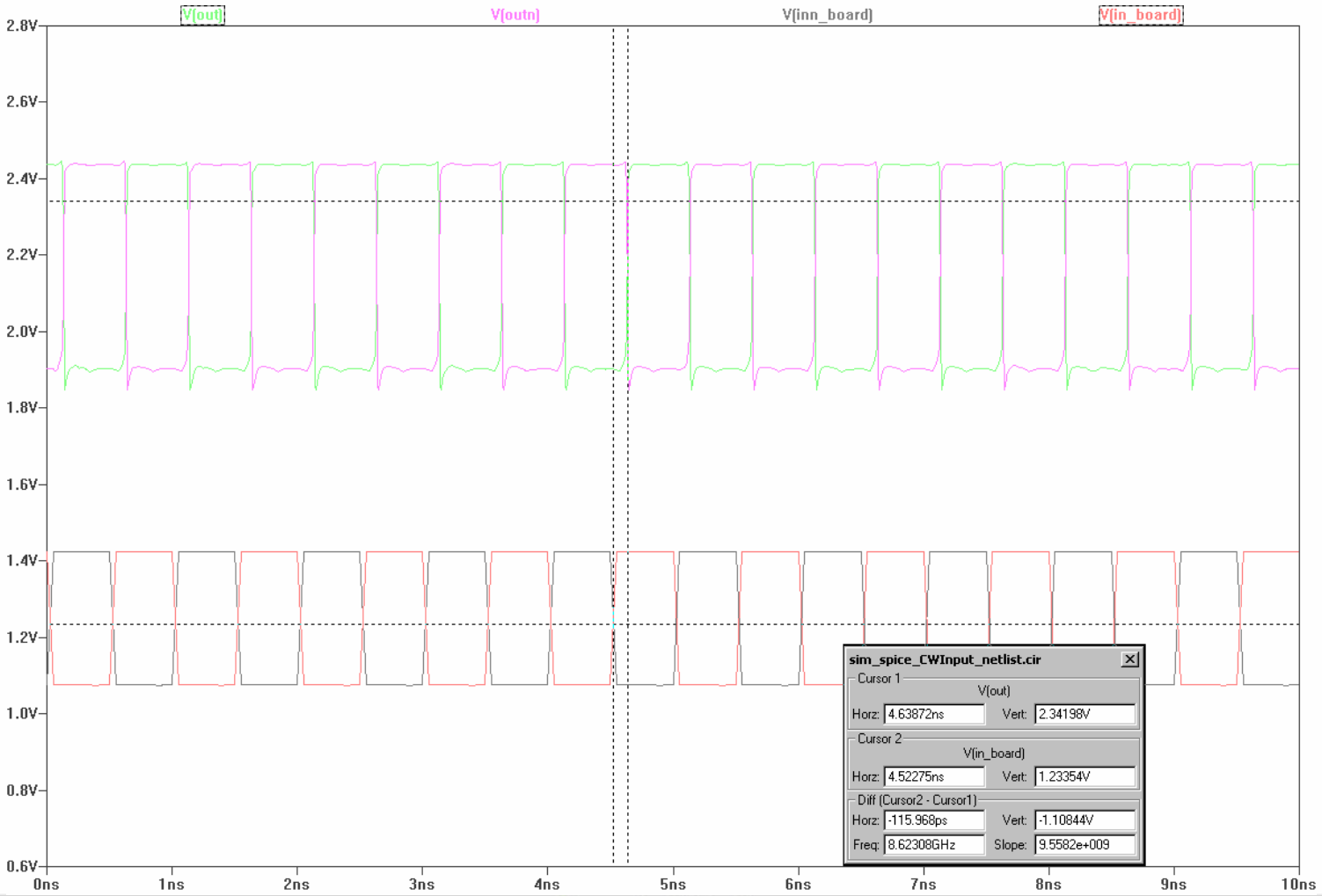
CW Clock Input Buffer Schematic



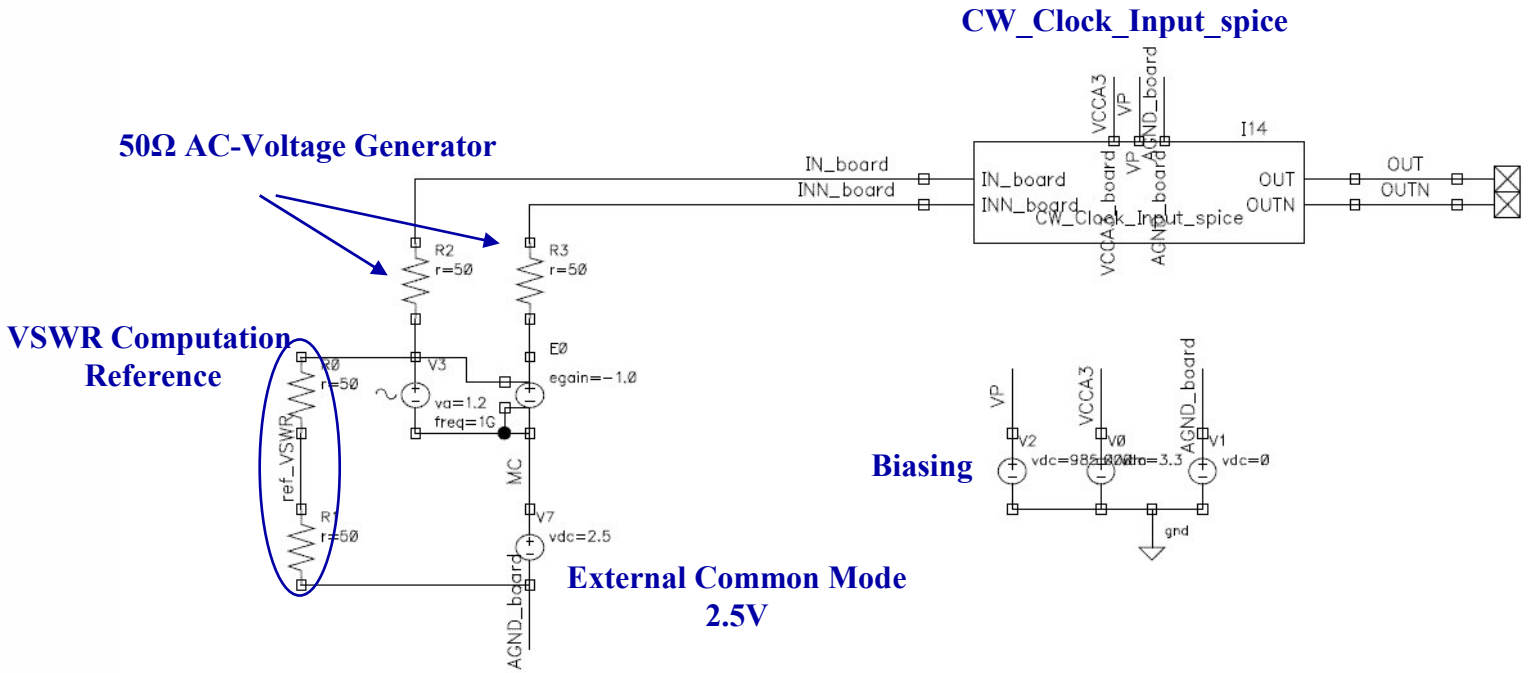
Clock Input Transient Response (Spectre) @27°C; 1GHz



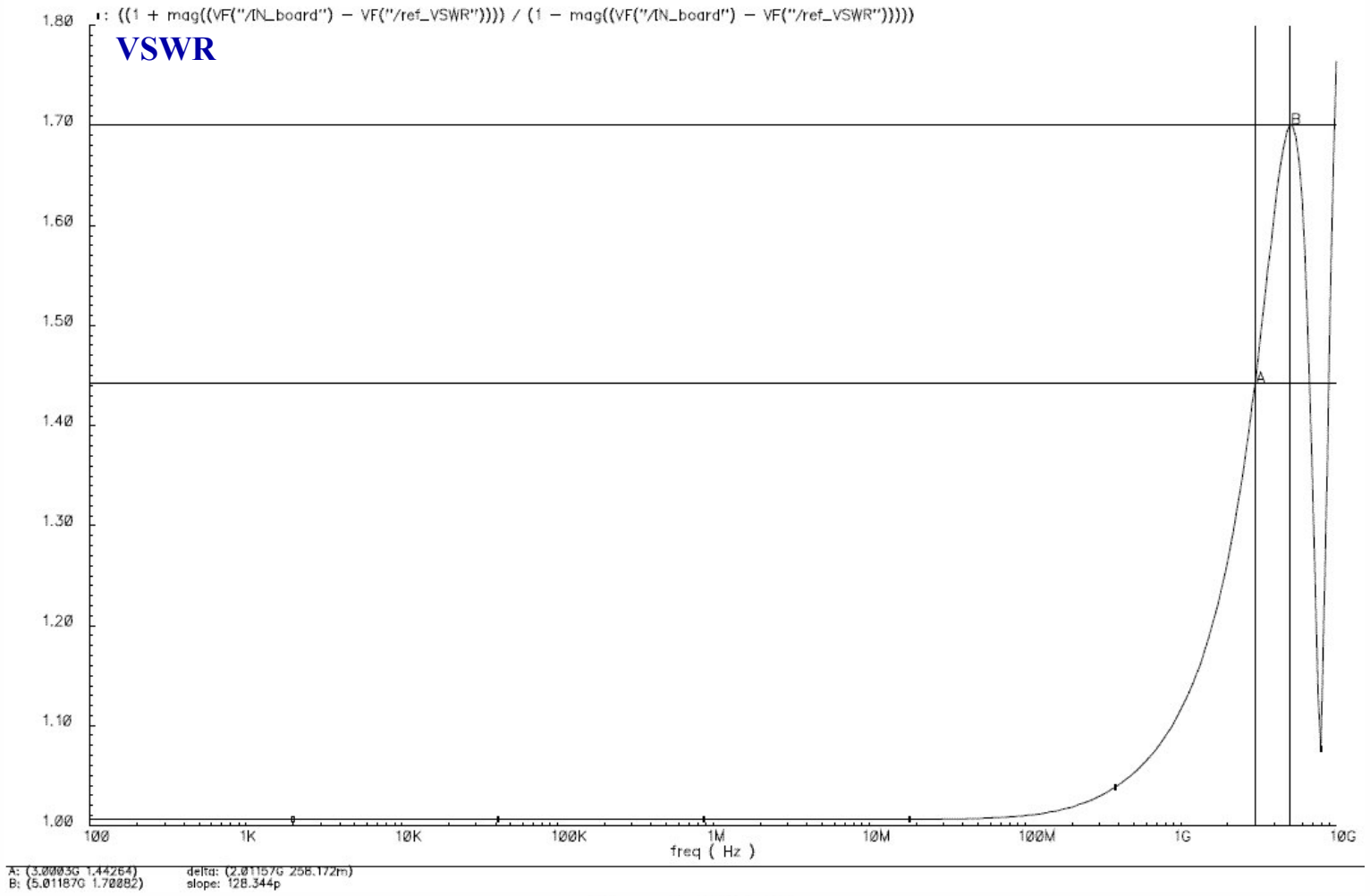
Clock Input Transient Response (Spice) @27°C; 1GHz



Top Level Simulation Schematic (VSWR)



Clock Input VSWR Response (Spectre) @27°C; from 100Hz to 10GHz



Clock Input VSWR Response (Spice) @27°C; from 100Hz to 10GHz