EV12DS130

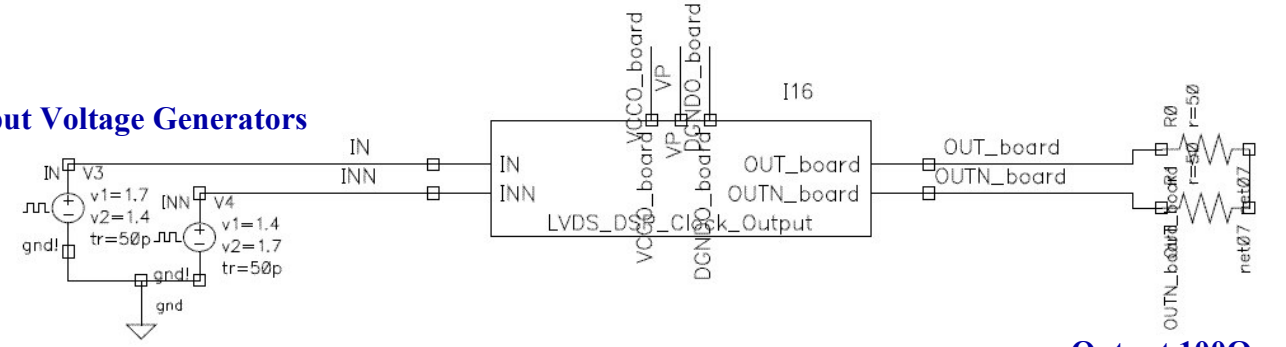
Spice Models

LVDS DSP Clock Output Buffer (transient)

Top Level Simulation Schematic (Transient)

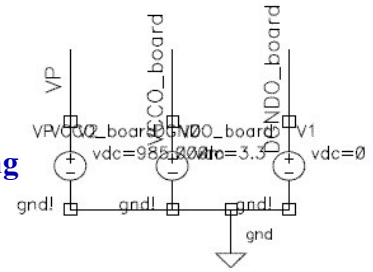
LVDS_DSP_Clock_Output
(described hereafter)

Input Voltage Generators



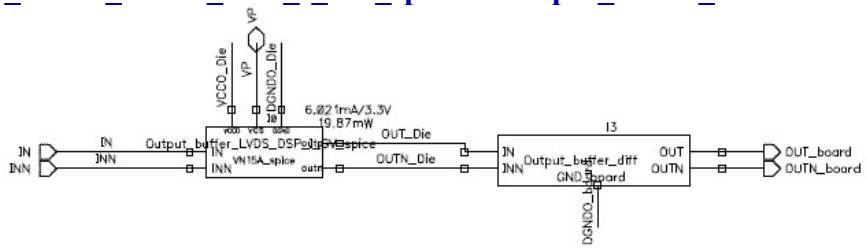
Output 100Ω
Differential Load

Biasing

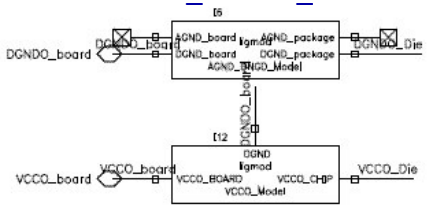


TOP LVDS DSP Clock Output Schematic

Output_buffer_LVDS_DSP_I_GV_spice **Output_buffer_diff**



AGND_DGND_Model



VCCO_Model

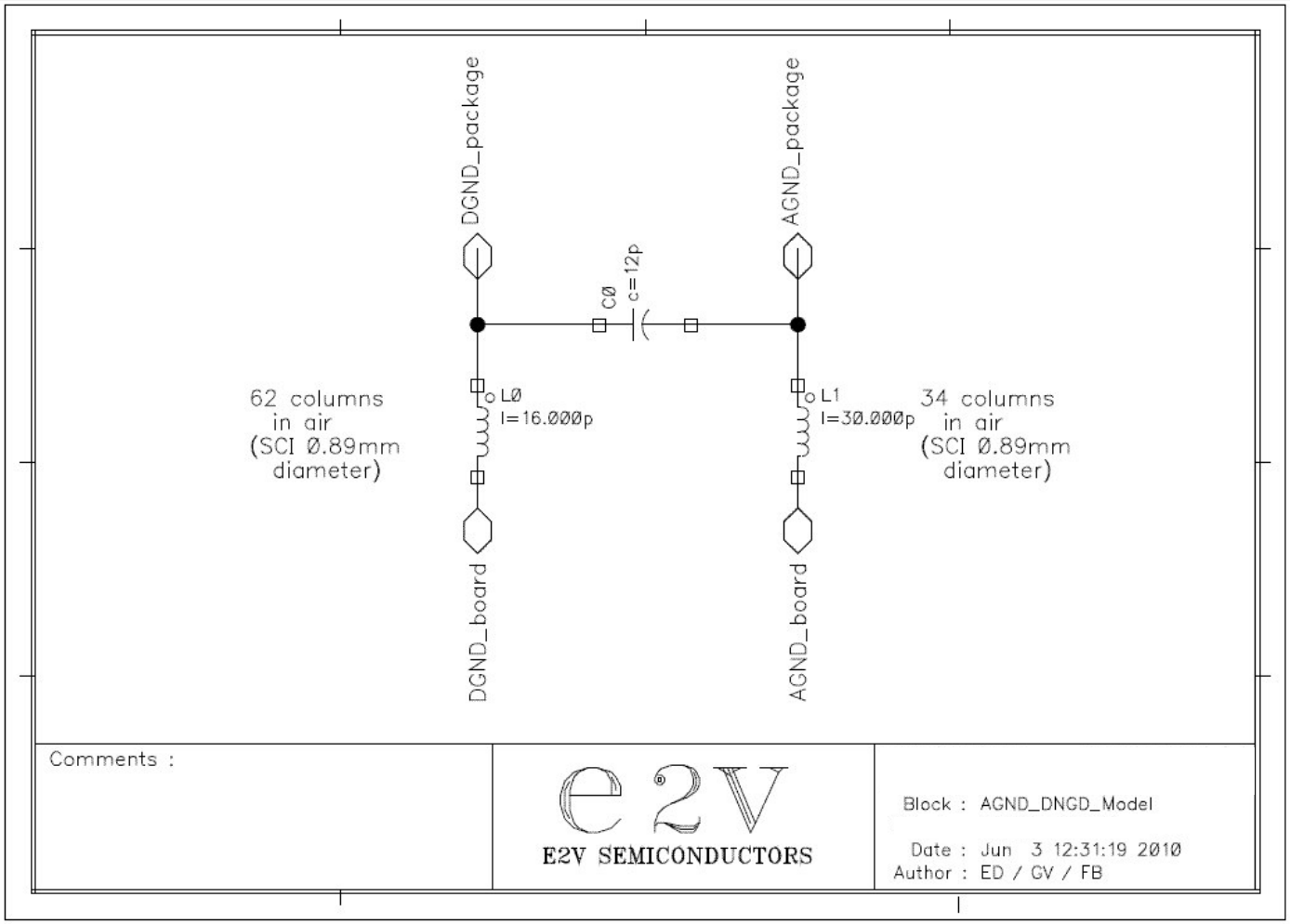
Comments :
DSP Clock Output Buffer with
– Differential Output Transmission Lines
– Power Supply and Ground Package Models

E2V SEMICONDUCTORS

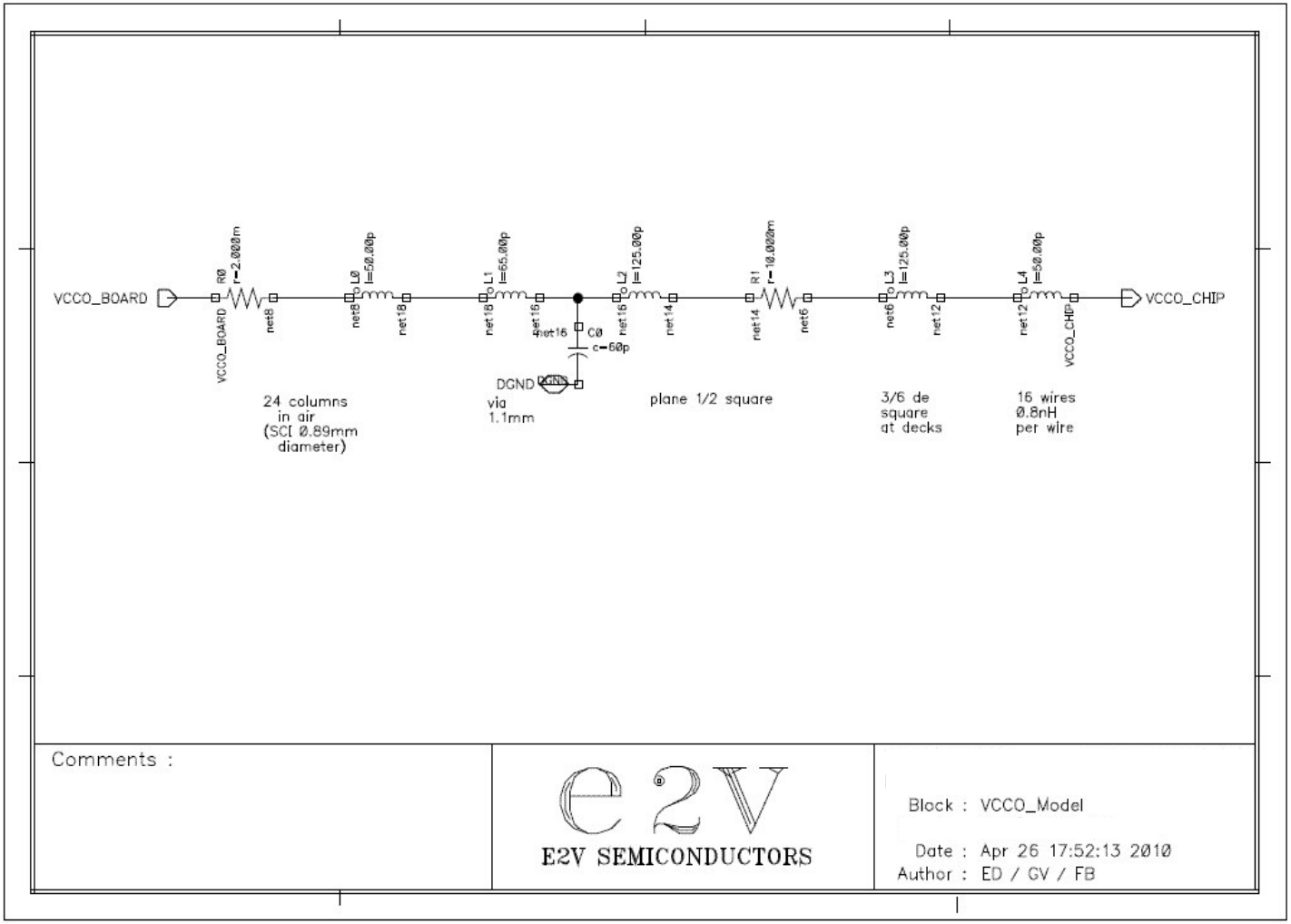
Block : LVDS_DSP_Clock_Output

Date : Jun 1 17:29:49 2010
Author : ED / GV / FB

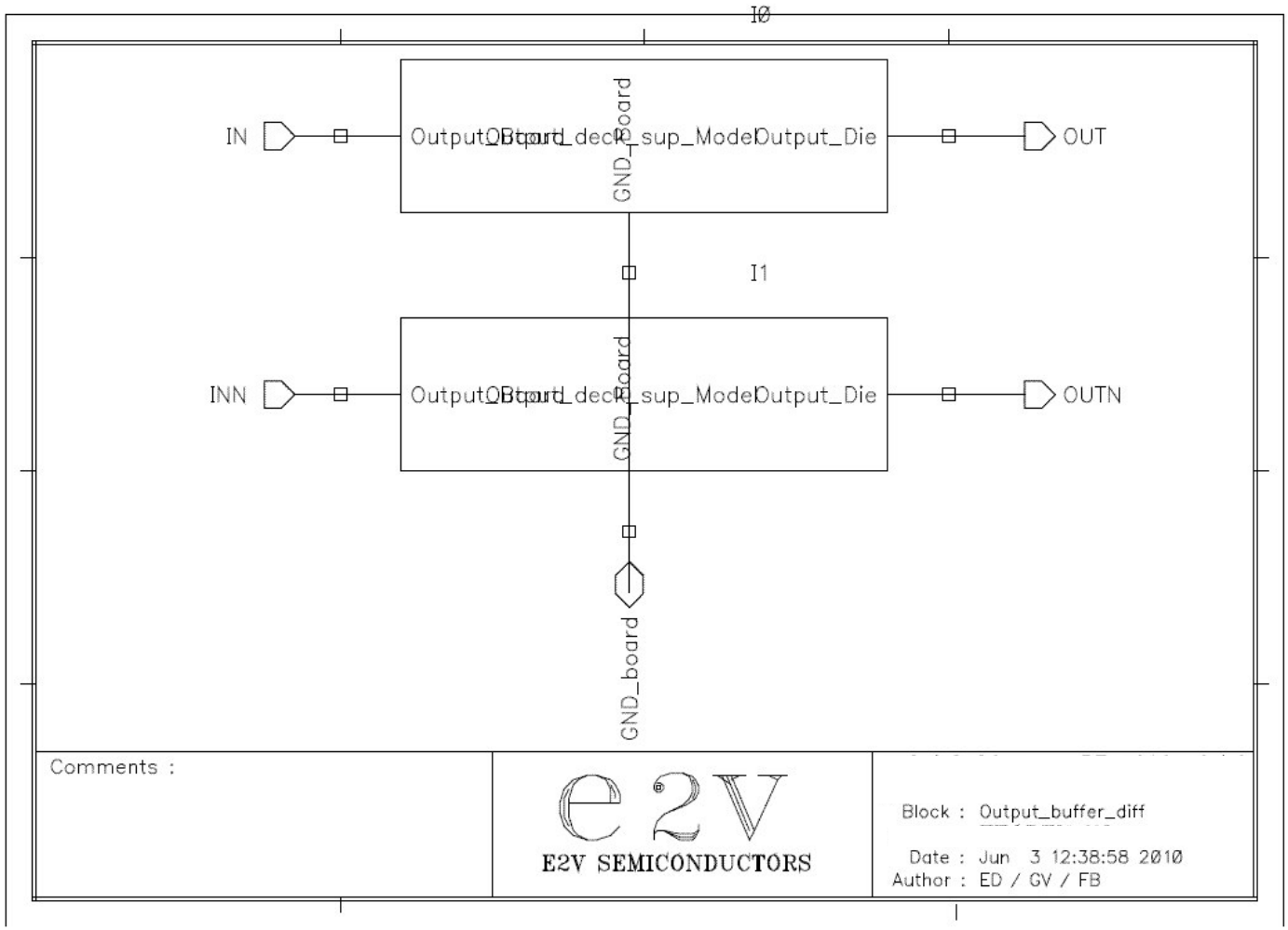
Ground Package Model
AGND & DGND



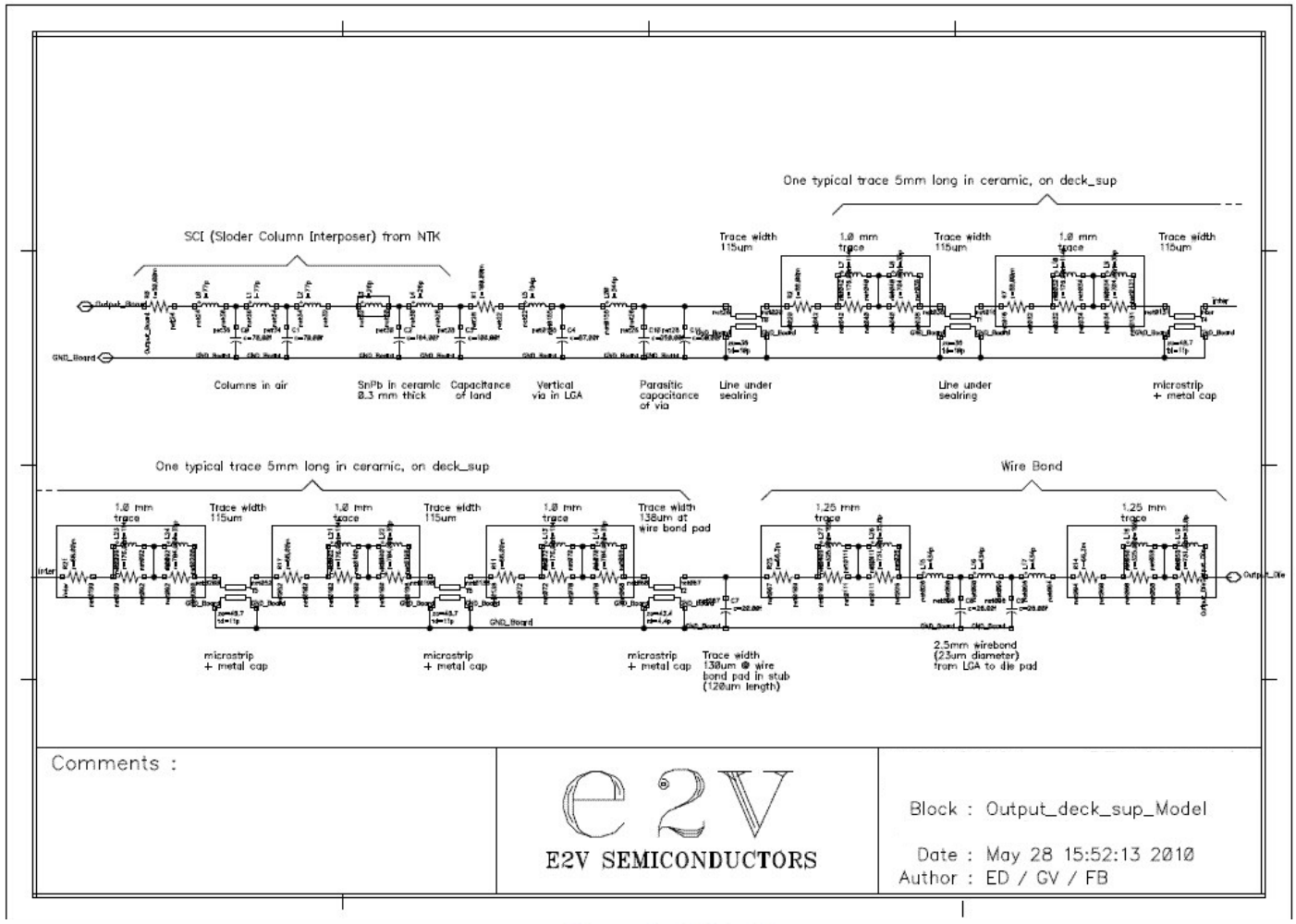
Power Supply Package Model
VCCO



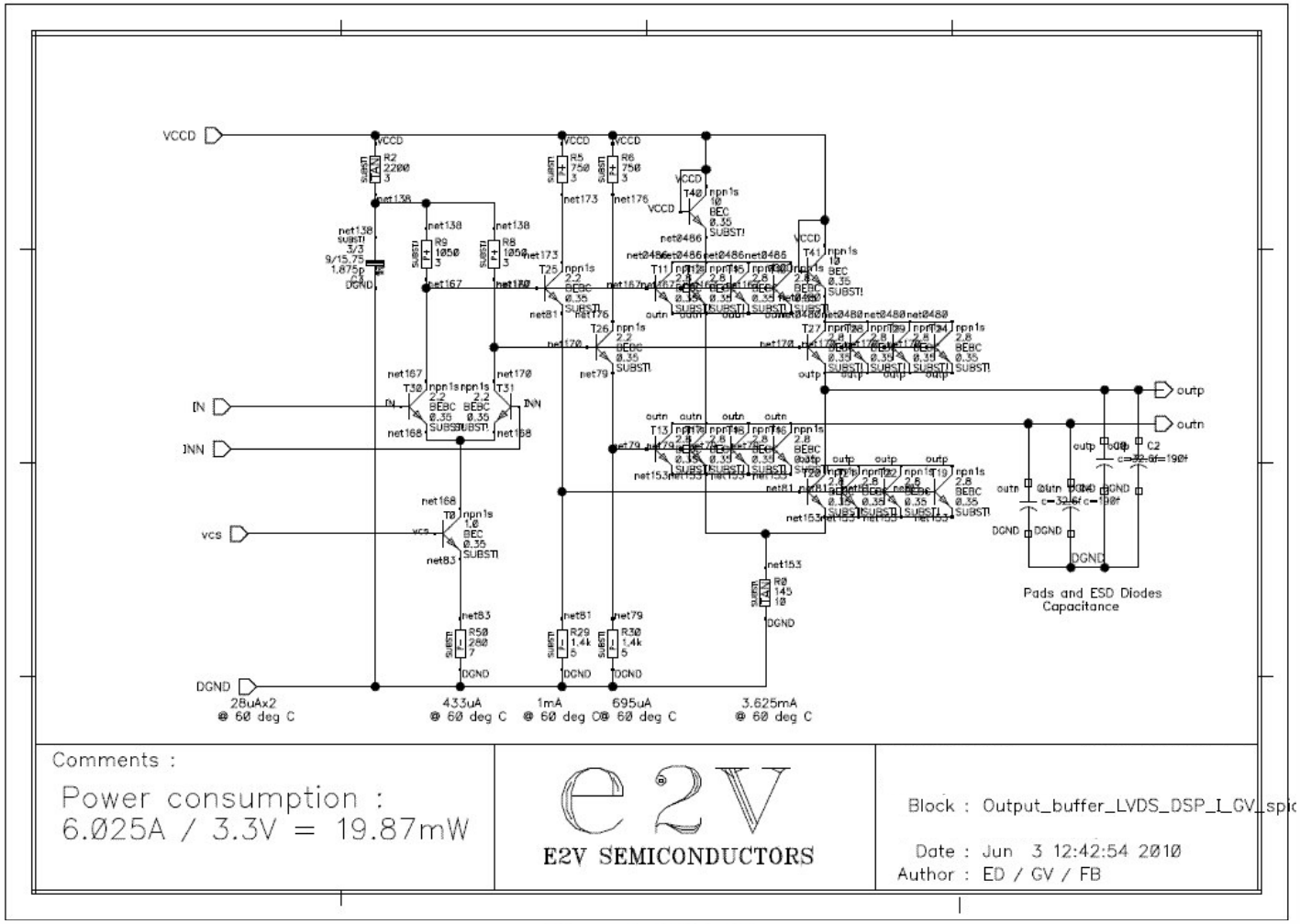
I/O Lines Package Models in Differential



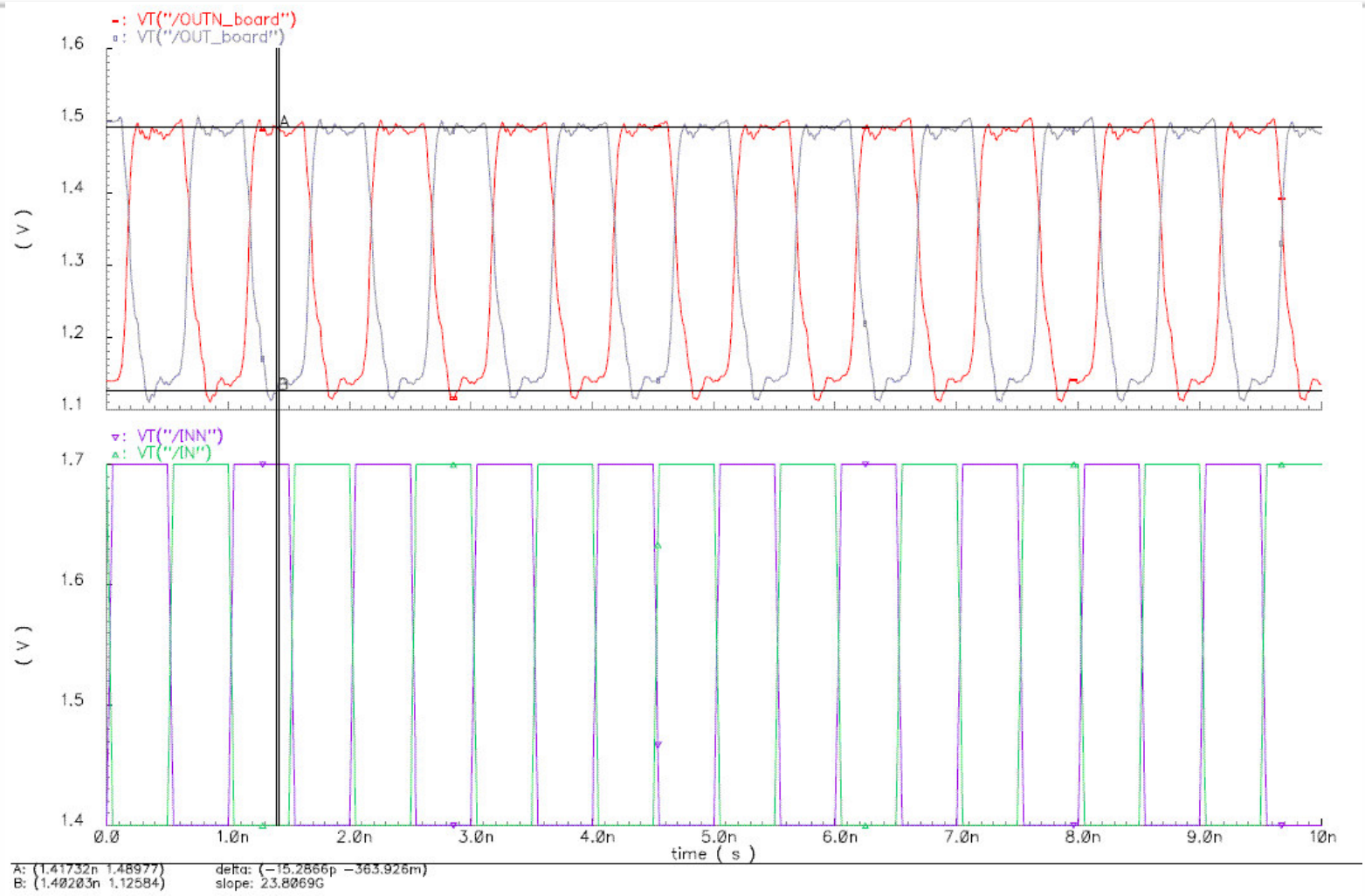
I/O Lines Package Model Single



LVDS DSP Clock Output Buffer Schematic



DSP Clock Output Transient Response (Spectre) @27°C; 1GHz



DSP Clock Output Transient Response (Spice) @27°C; 1GHz